专用集成电路设计

ASIC Design

西安电子科技大学　XIDIDIAN UNIVERSITY
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本次课主题：MOSIC版图

本次课内容

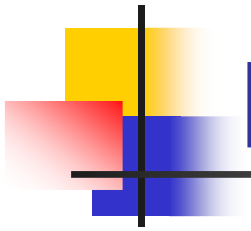
P-MOS和N-MOS基本版图

- 1. MOSFET
- 2. 基本掩膜层
- 3. 源/漏接触
- 4. 多晶与栅氧
- 5. 多晶与金属
- 6. 多晶作互连线
- 7. 自对准栅
- 8. 共享扩散
- 9. 接触孔
- 10. 金属1
- 11. 通孔和金属2

简单门电路版图设计

- 1. 版图说明
- 2. CMOS反相器
- 3. CMOS与非门
- 4. CMOS或非门
- 5. CMOS传输门
- 6. CMOS AOI门
- 7. CMOS OAI门
- 8. 2输入选择器
- 9. CMOS触发器

标准单元版图



Layout show

- 见word文件
- 标准单元show(见tbd文件)

P-MOS和N-MOS基本版图

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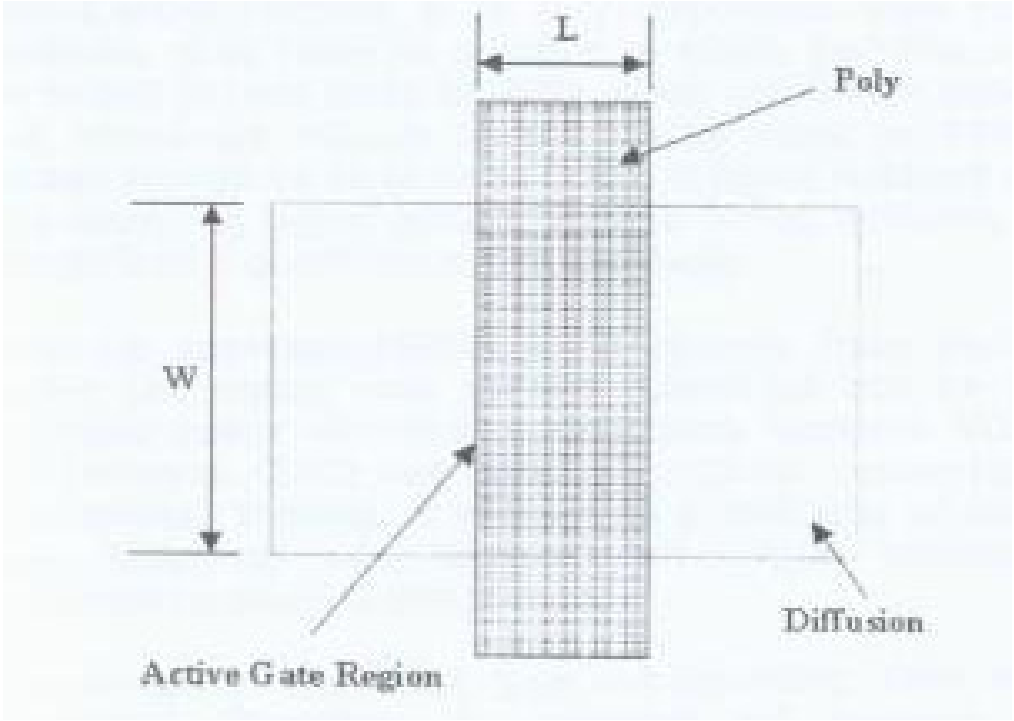
- 11. 通孔和金属2

基本版图——1. MOSFET

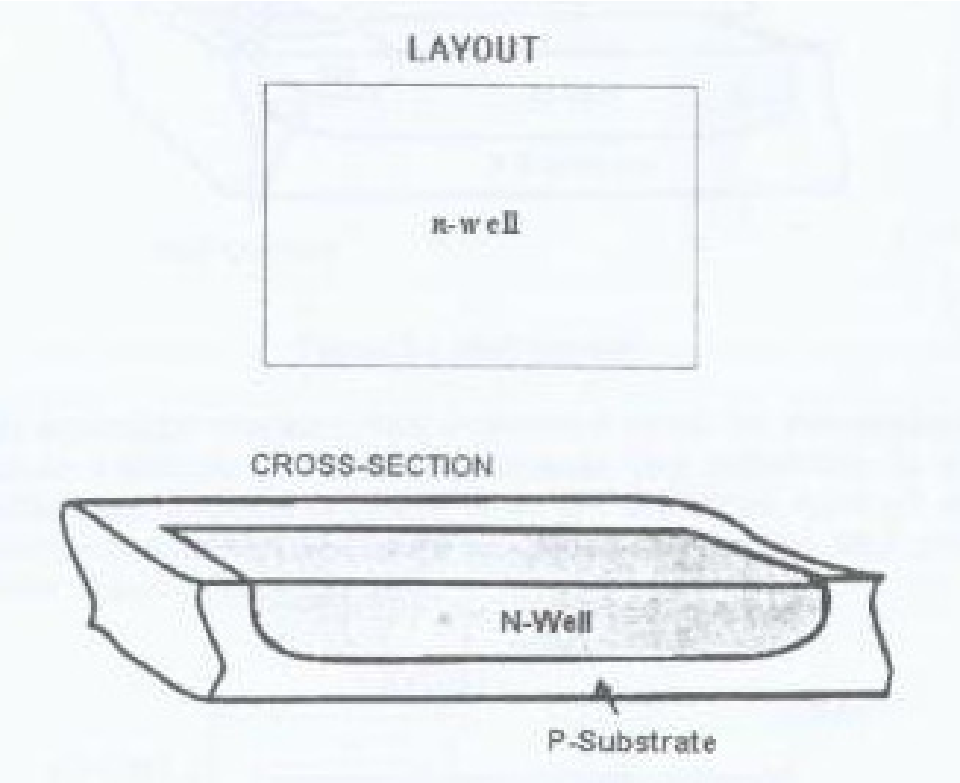
- W
- L

- 三个电极
  - 源S漏D栅 G



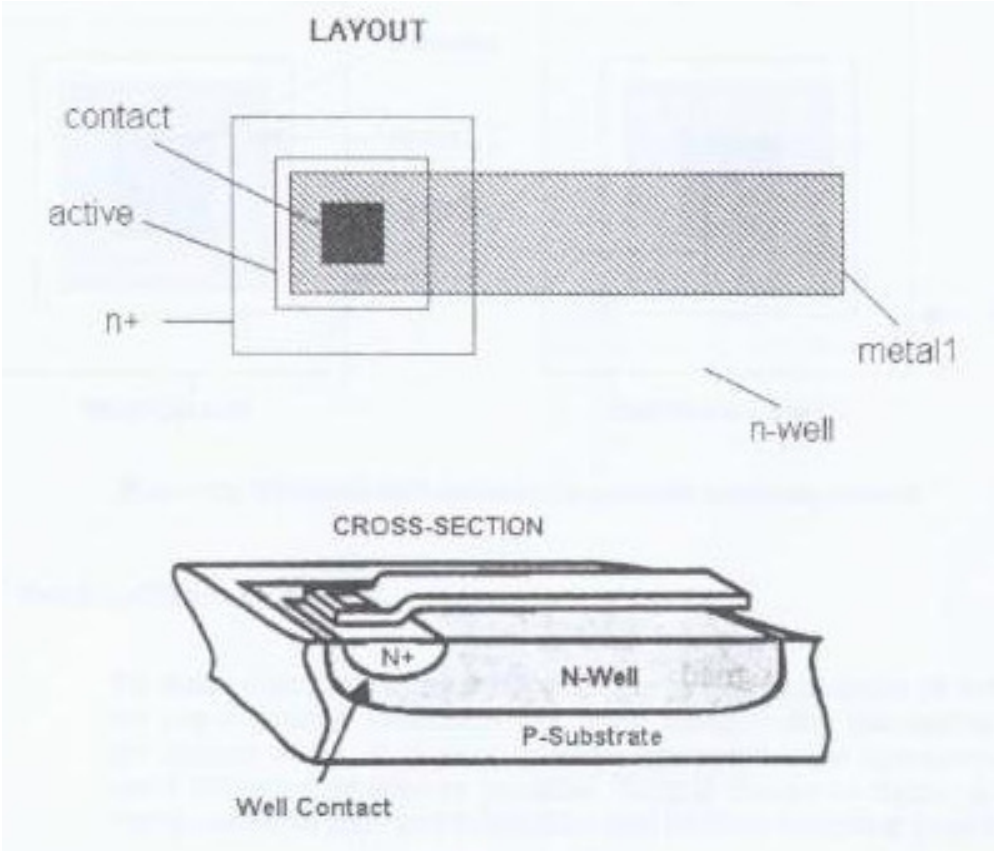
基本版图——2. 基本掩膜层

- (1) 阱扩散



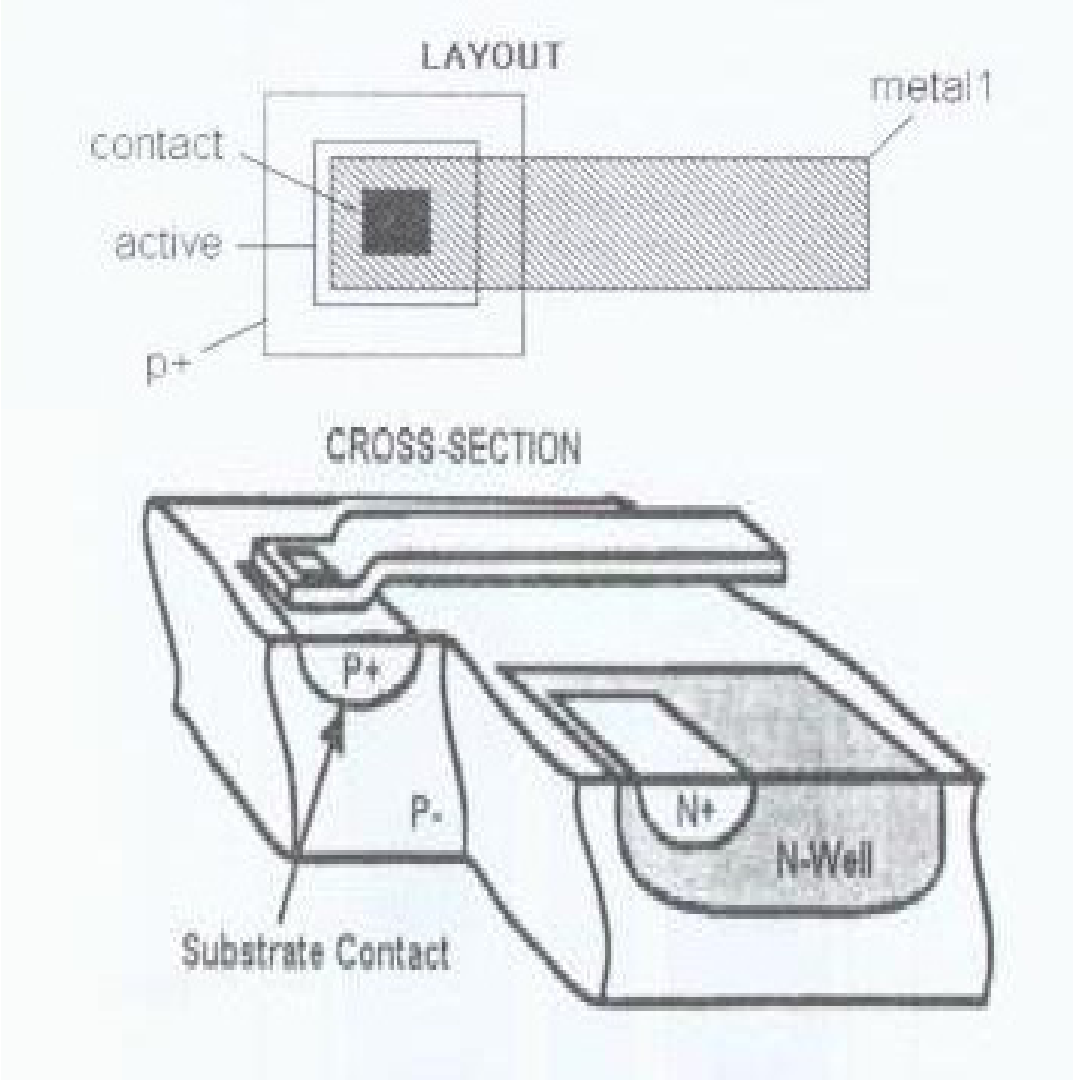
基本版图——2. 基本掩膜层

- (2) 阱接触

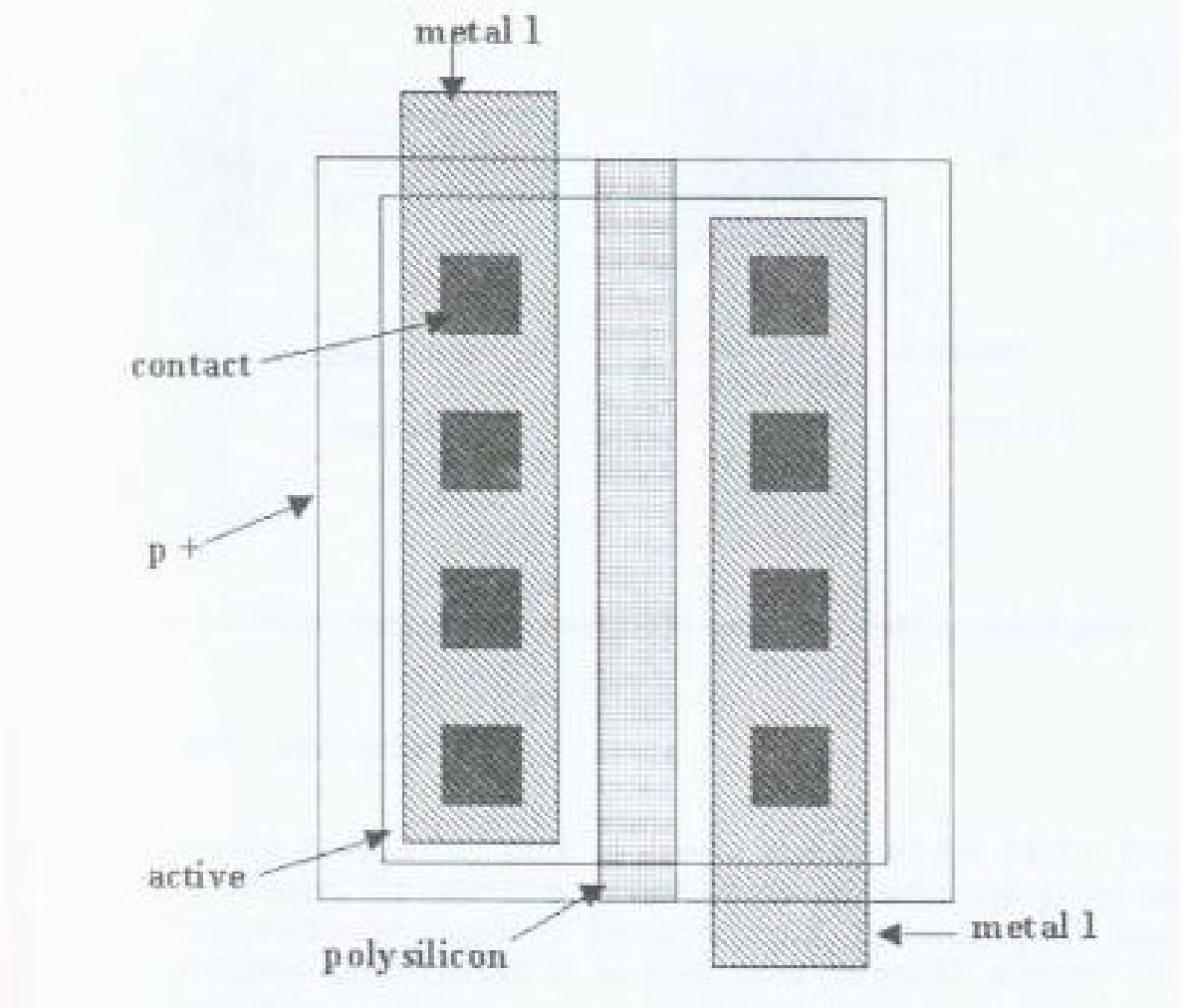


基本版图——2. 基本掩膜层

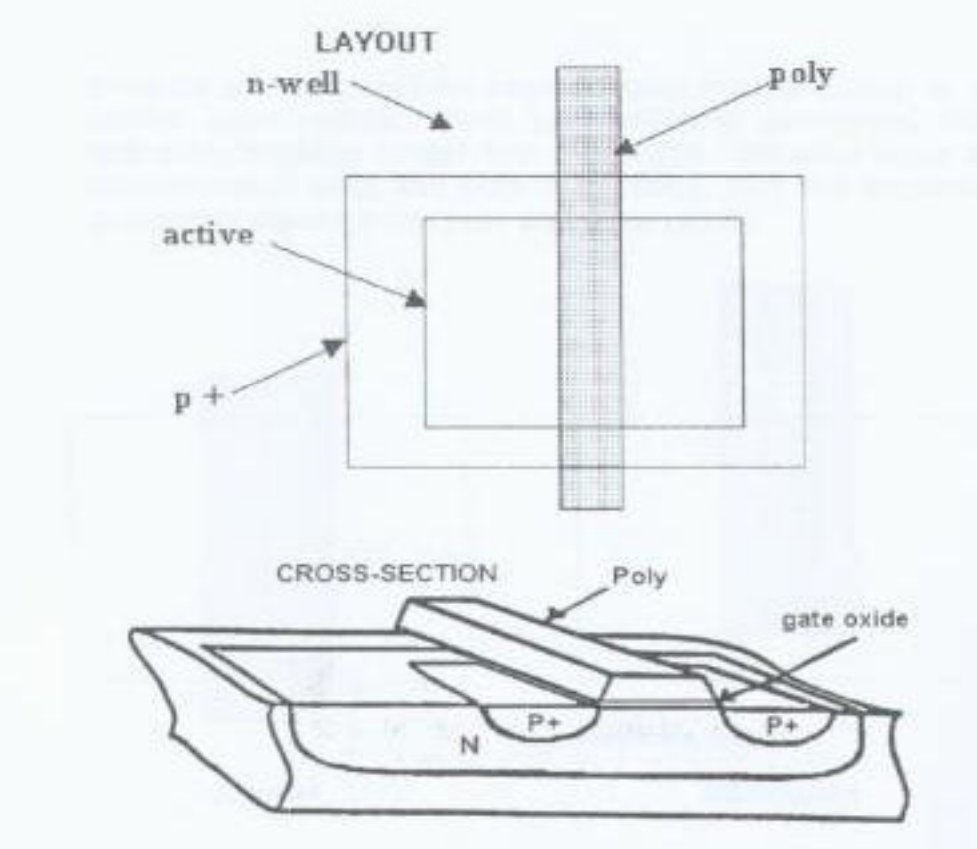
- (3)衬底接触



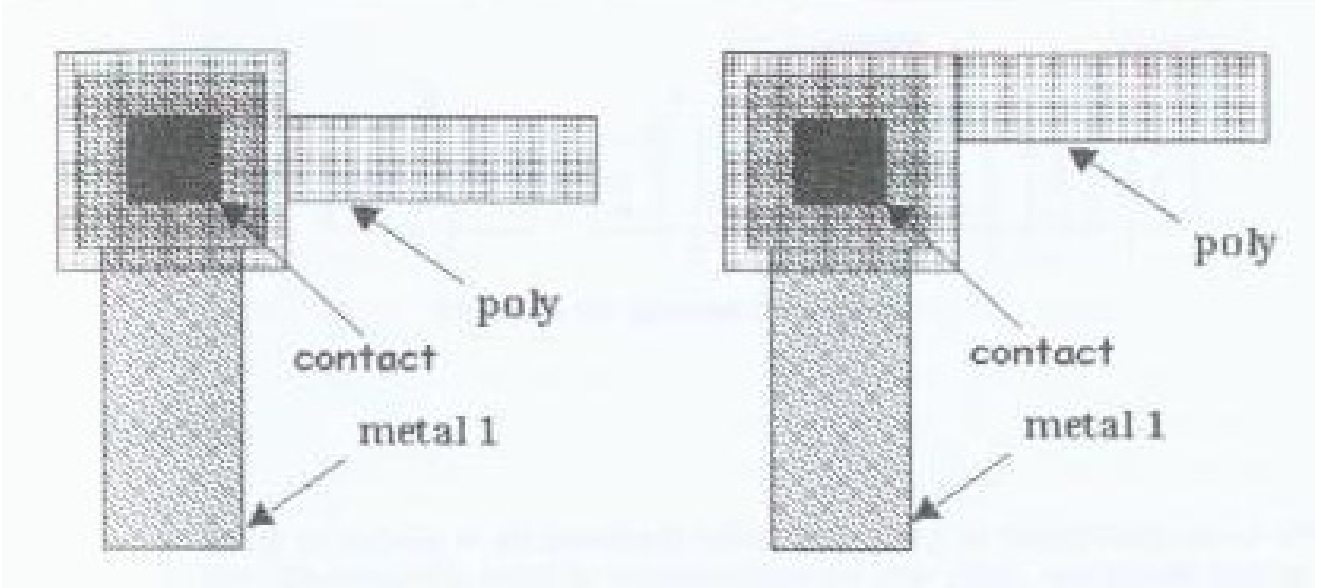
基本版图——3. 源/漏接触



基本版图——4. 多晶与栅氧

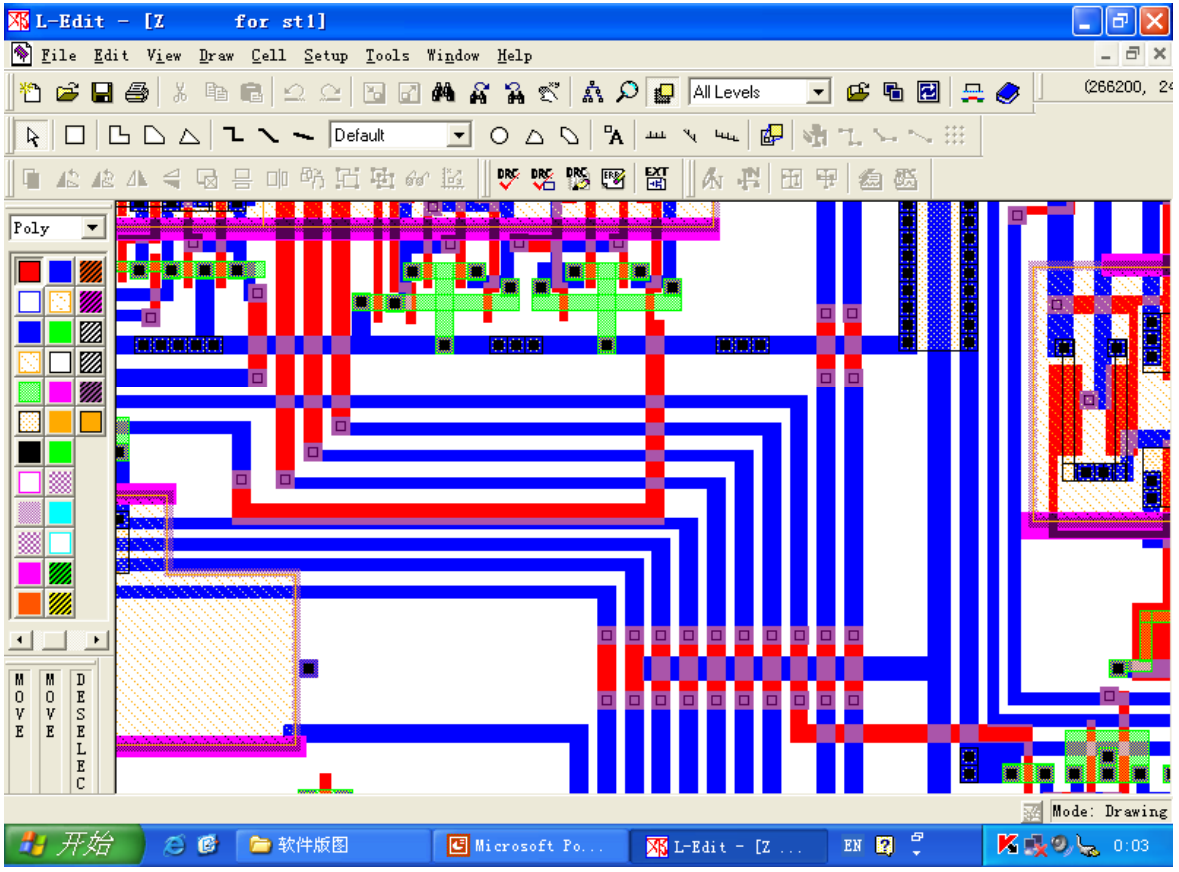

LAYOUT
n-well
poly
active
p +
CROSS-SECTION
Poly
gate oxide
P+
P+
N

基本版图——5. 多晶与金属



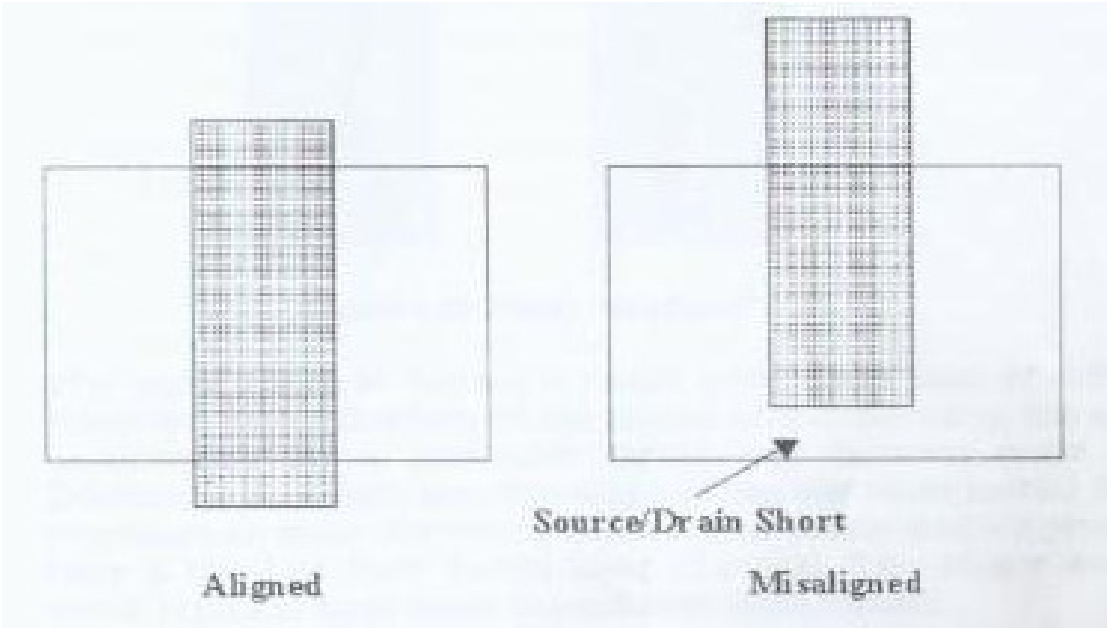
基本版图——6. 多晶作互连线

- 双层布线

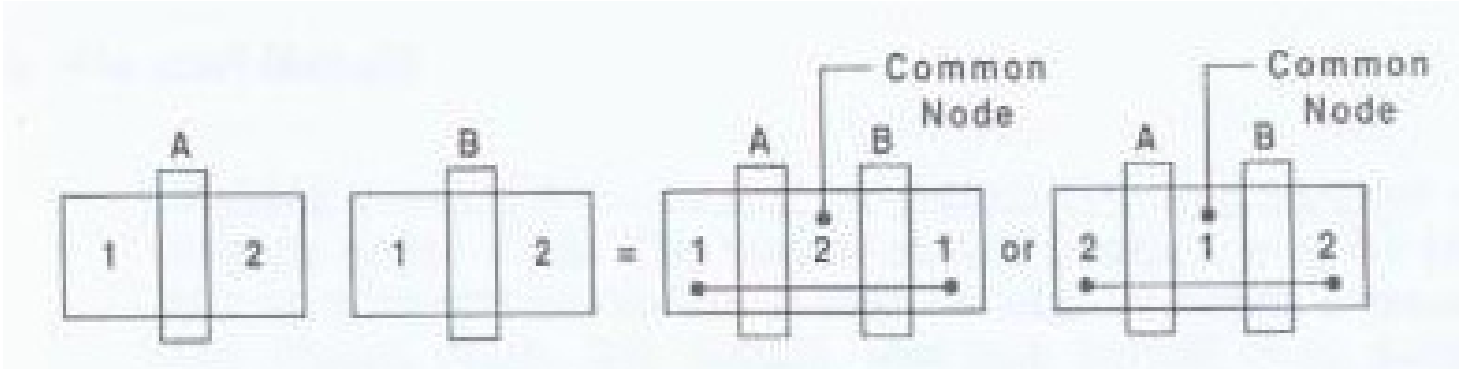


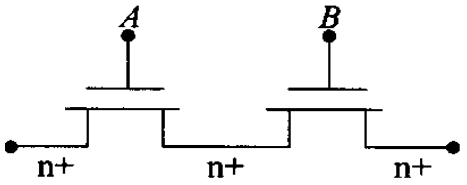
基本版图——7. 自对准栅

- 自对准

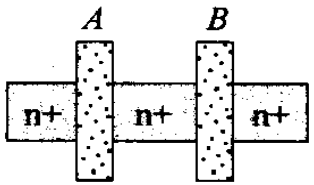


基本版图——8. 共享扩散

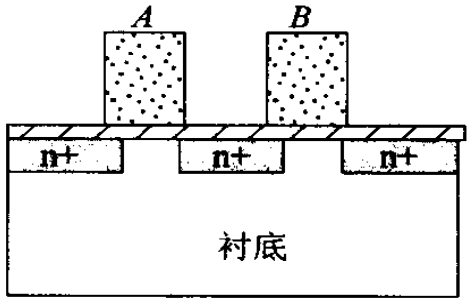




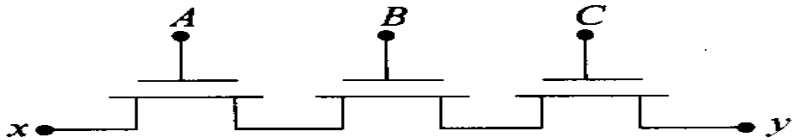
(a) 电路图



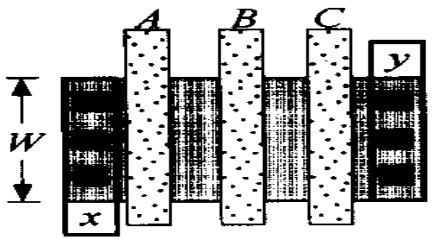
(b) 表面视图



(c) 侧视图



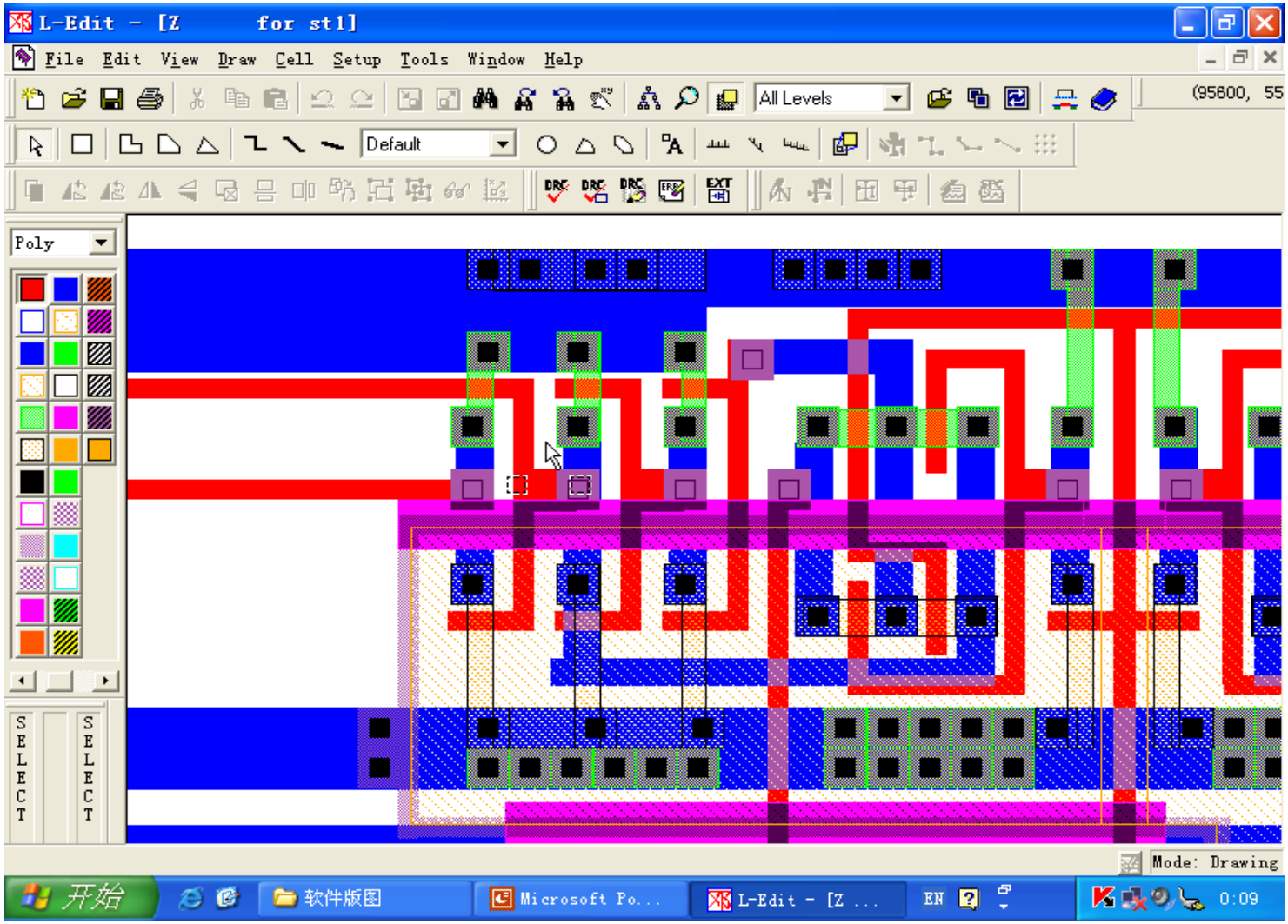
(a) 电路图



(b) 表面视图

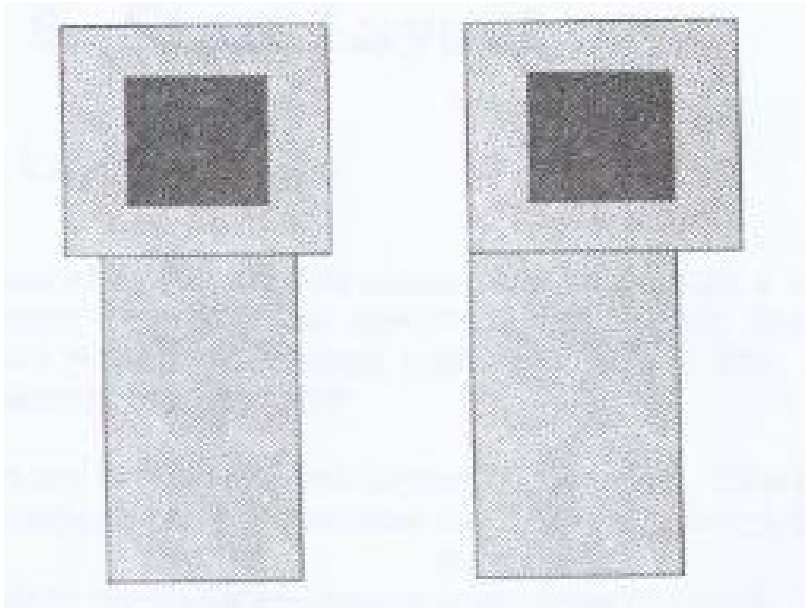
西

基本版图——9. 接触孔


L-Edit - [Z for st1]
File Edit View Draw Cell Setup Tools Window Help
All Levels
(95600, 55
Default
Poly
SELECT
SELECT
Mode: Drawing
开始
软件版图
Microsoft Po...
L-Edit - [Z ...
EN
0:09

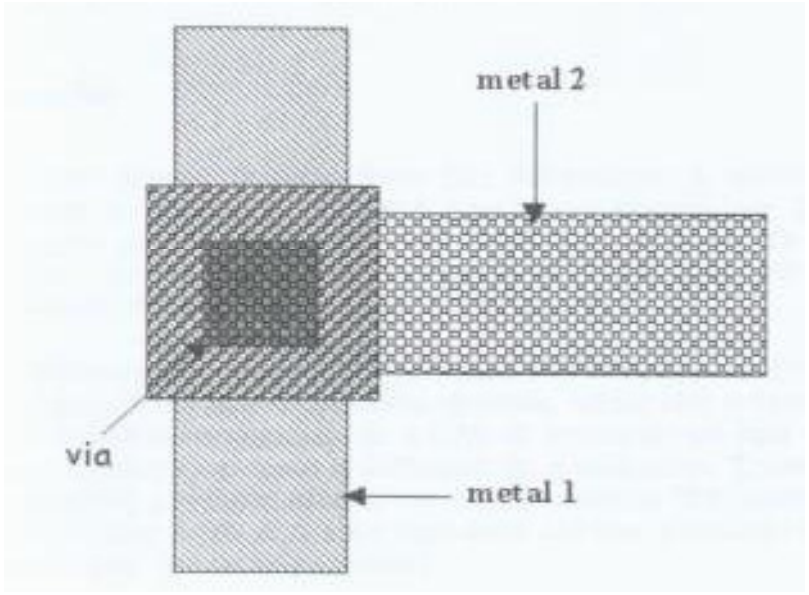
基本版图——10. 金属1

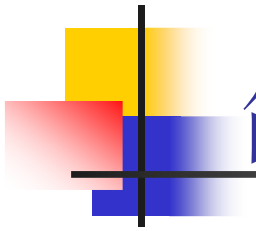
- 金属与下面N+或P+相连
- 金属与poly相连



基本版图——11. 通孔和金属2

- 两层金属相连





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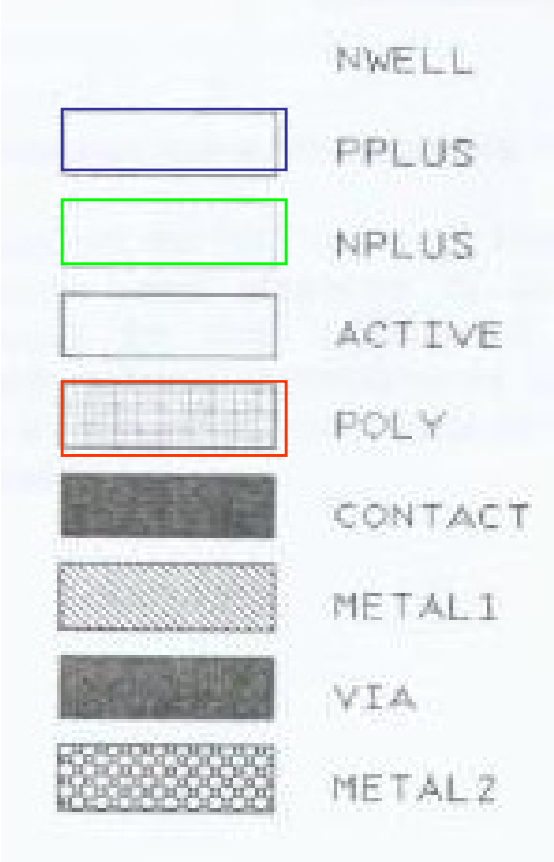
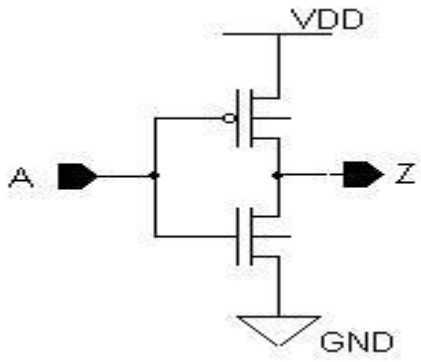
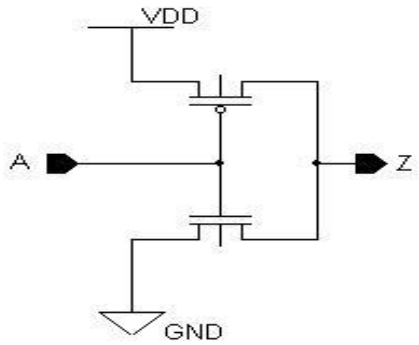
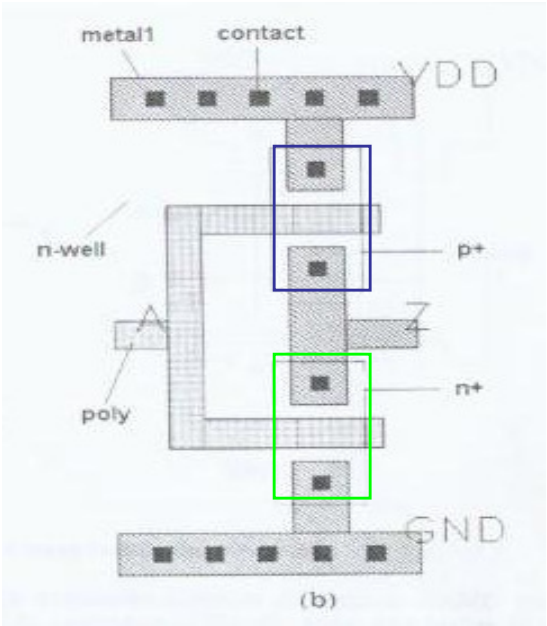
门电路版图——1. 版图说明

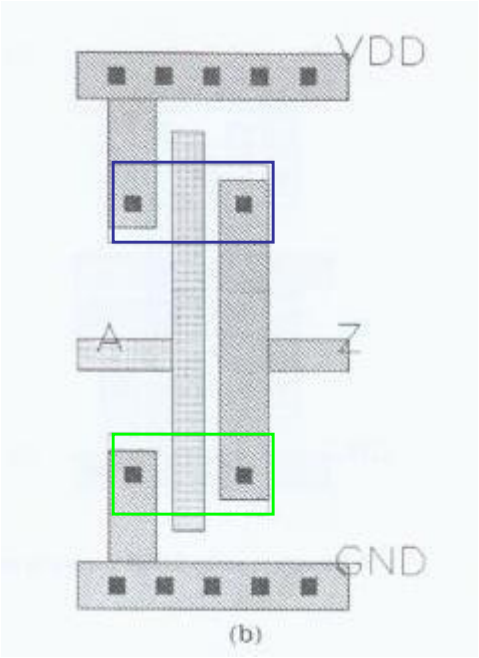


门电路版图——2. CMOS反相器

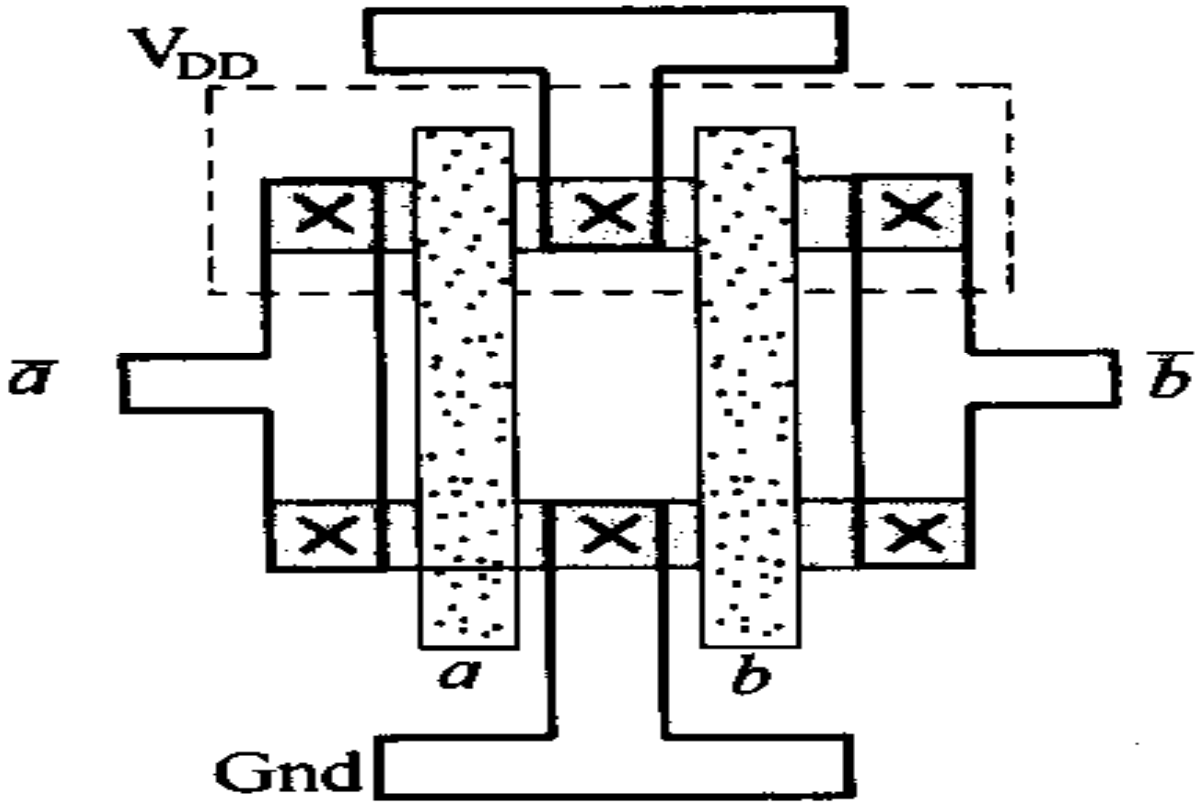




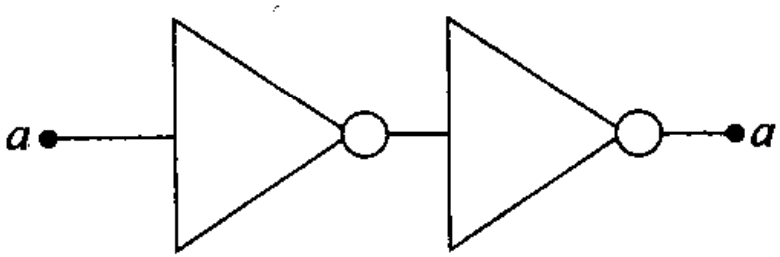


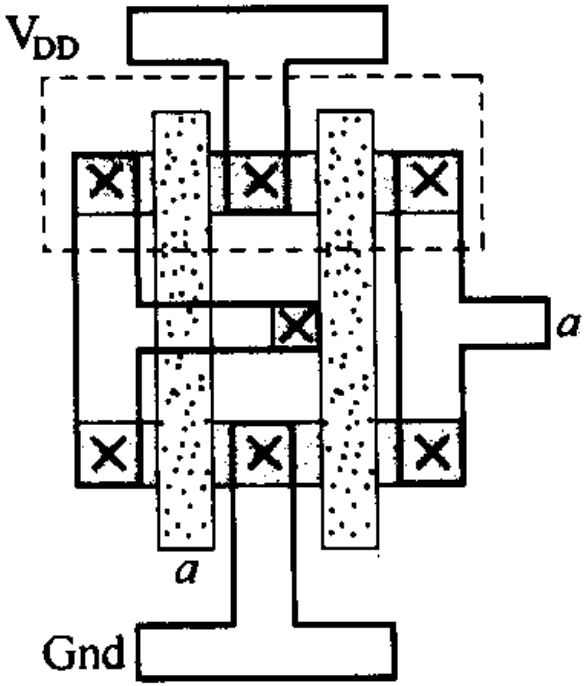


2个独立反相器

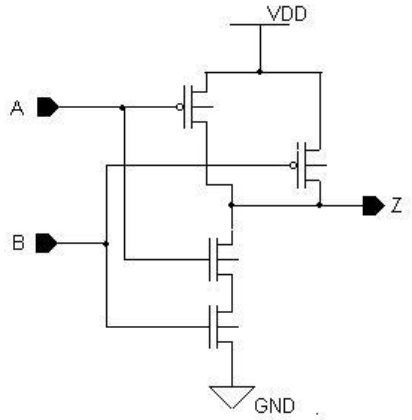


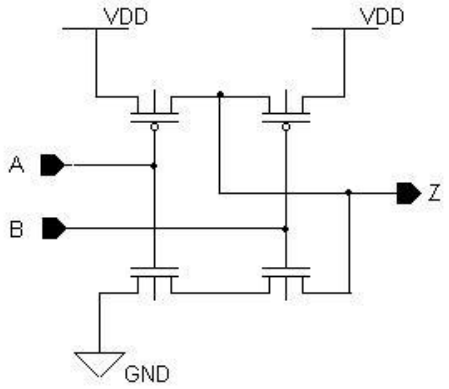
2个串联反相器

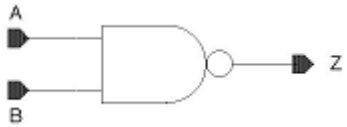


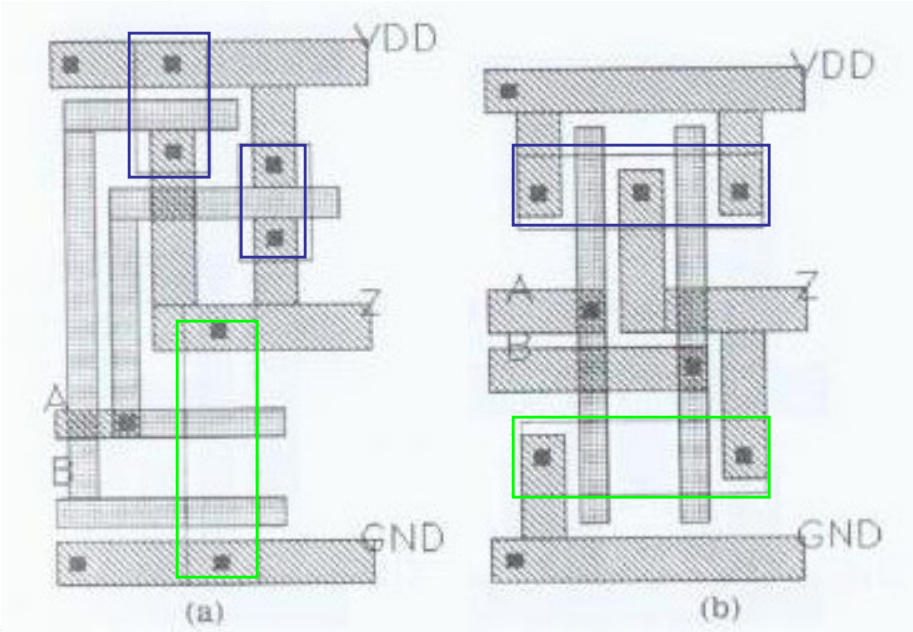


门电路版图——3. CMOS与非门



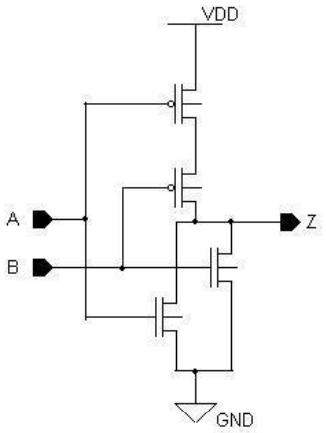


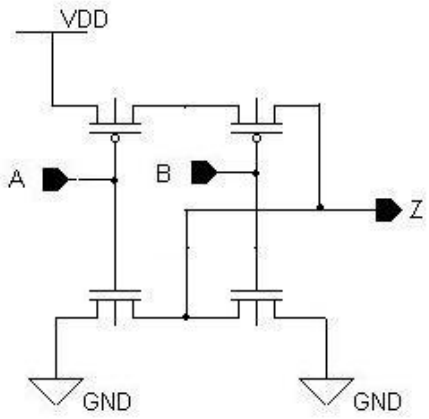


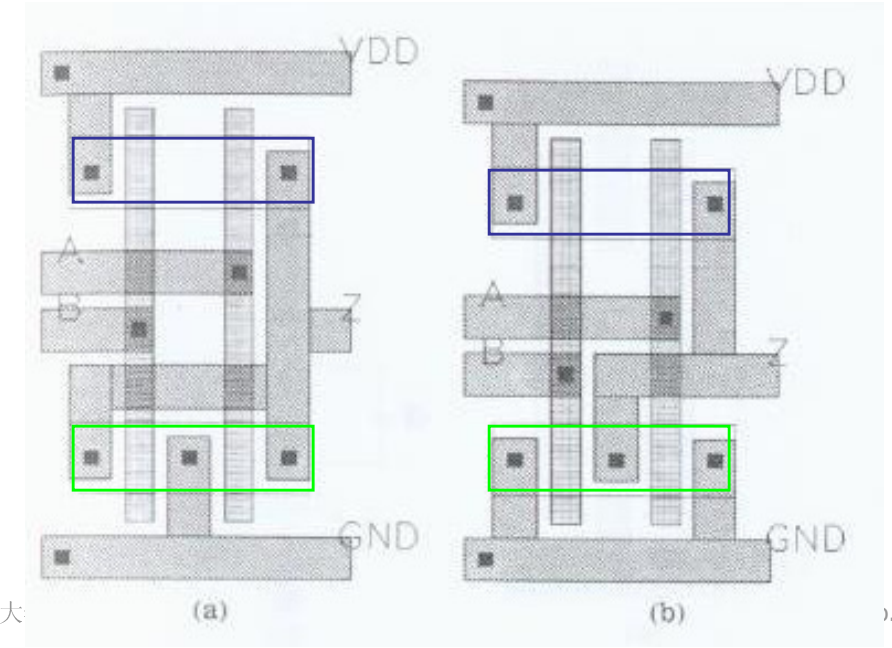


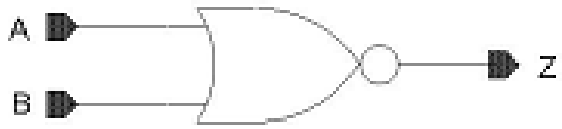
与非门: 全1得0 见0得1

门电路版图——4. CMOS或非门



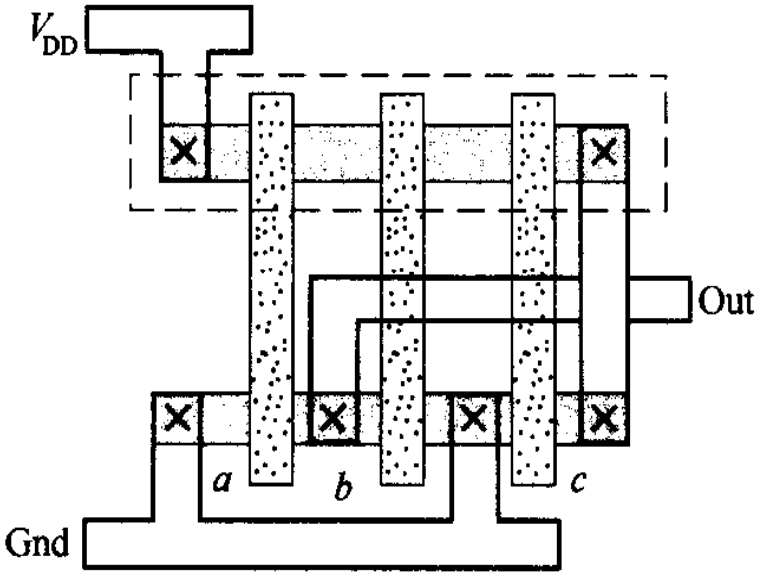




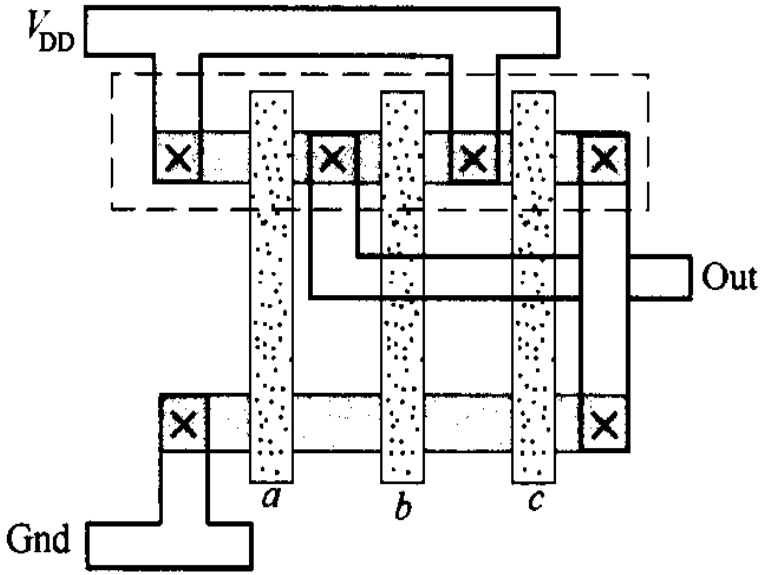


或非门: 全0得1 见1得0

NOR3/NAND3

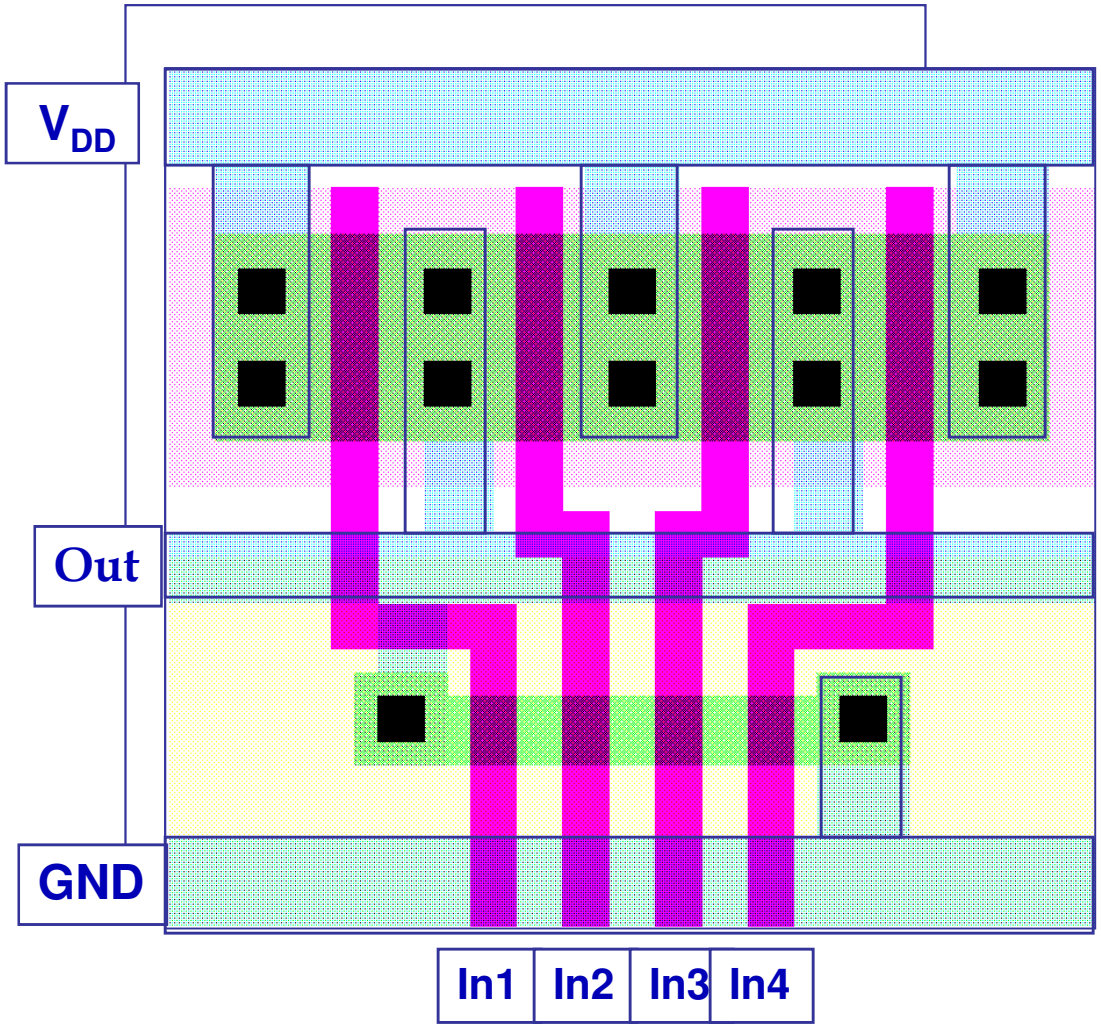


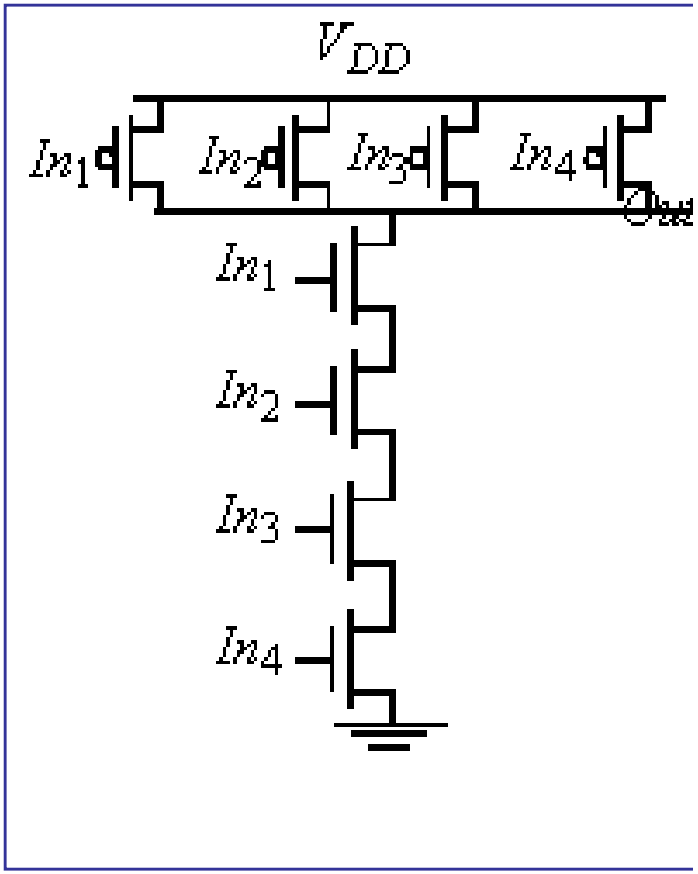
(a) NOR3



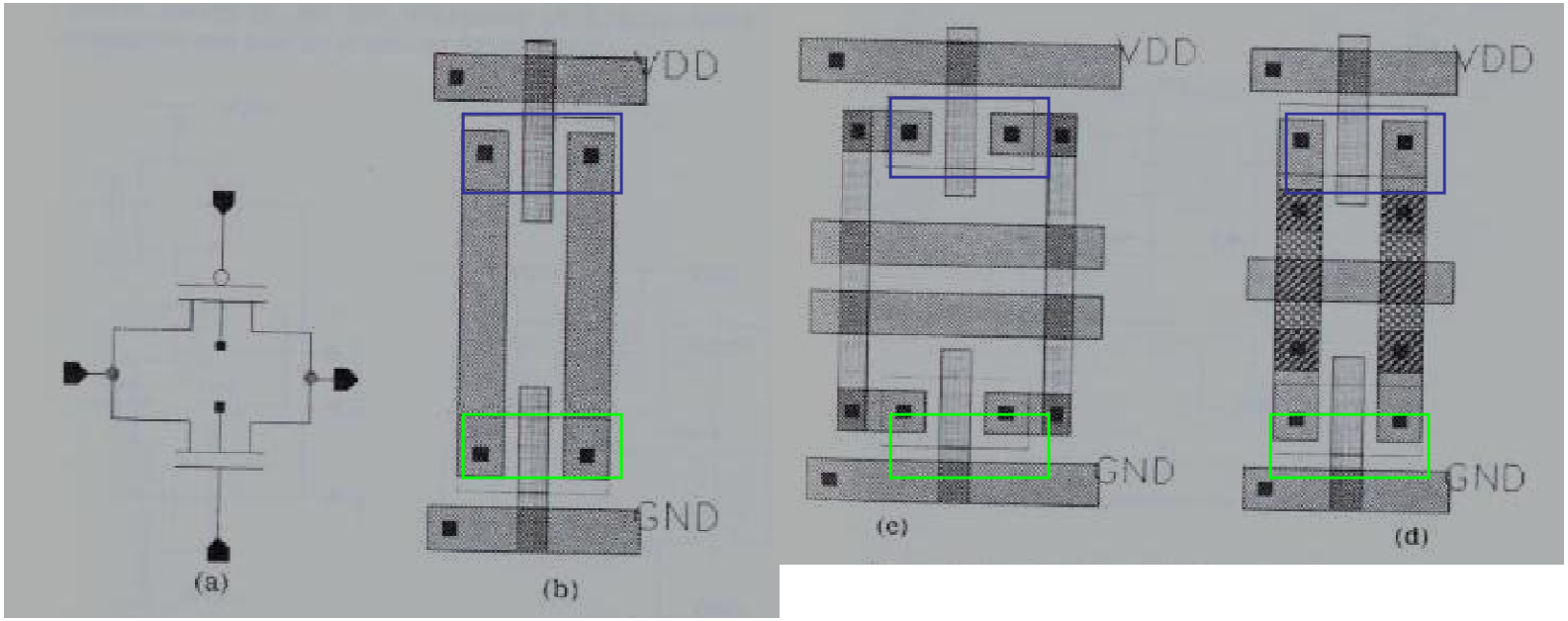
(b) NAND3

NAND4


VDD
Out
GND
In1
In2
In3
In4


VDD
In1
In2
In3
In4
Out
In1
In2
In3
In4

门电路版图——5. CMOS传输门

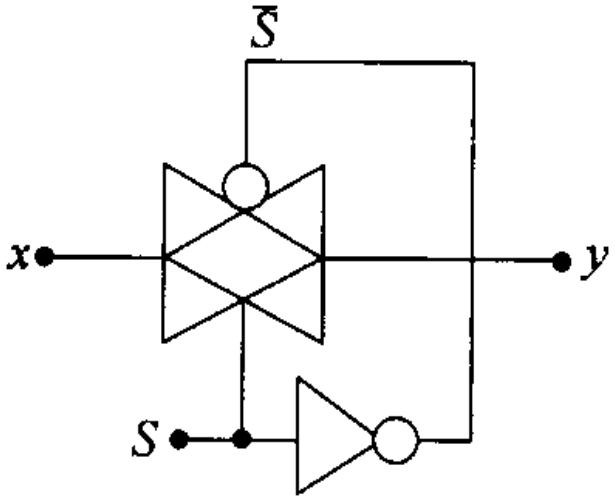


B金属过不去

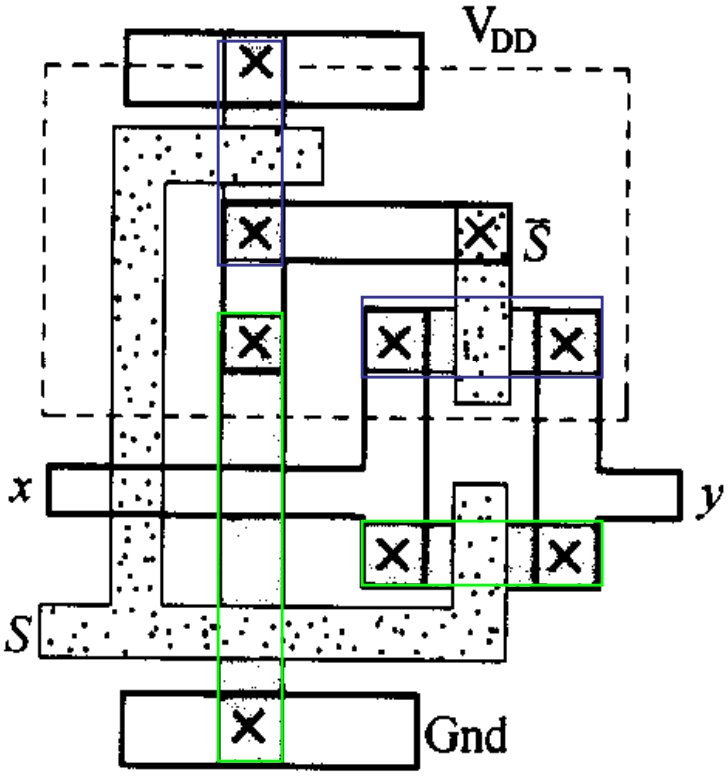
C太大

D双层

带反相驱动器的传输门

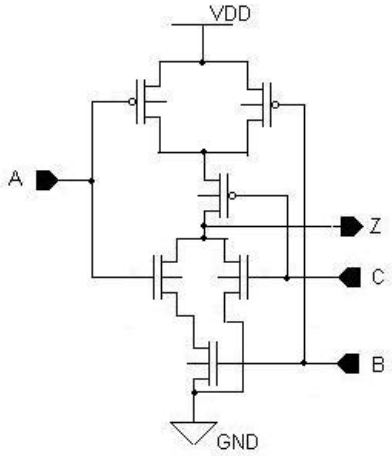


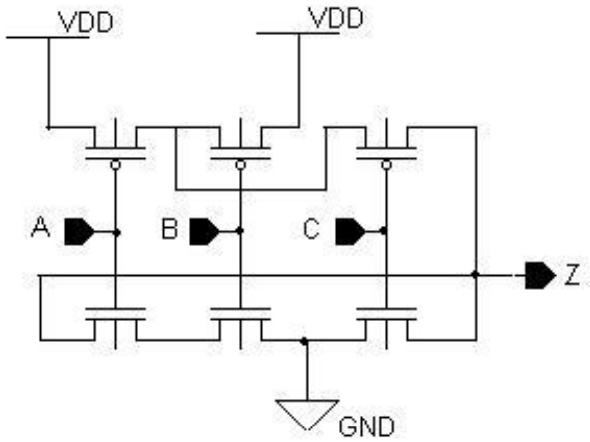
(a) 逻辑图

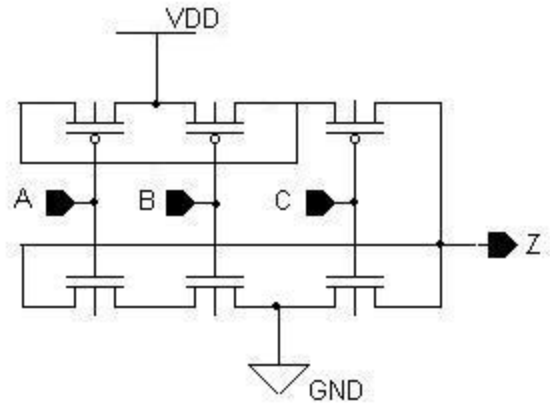


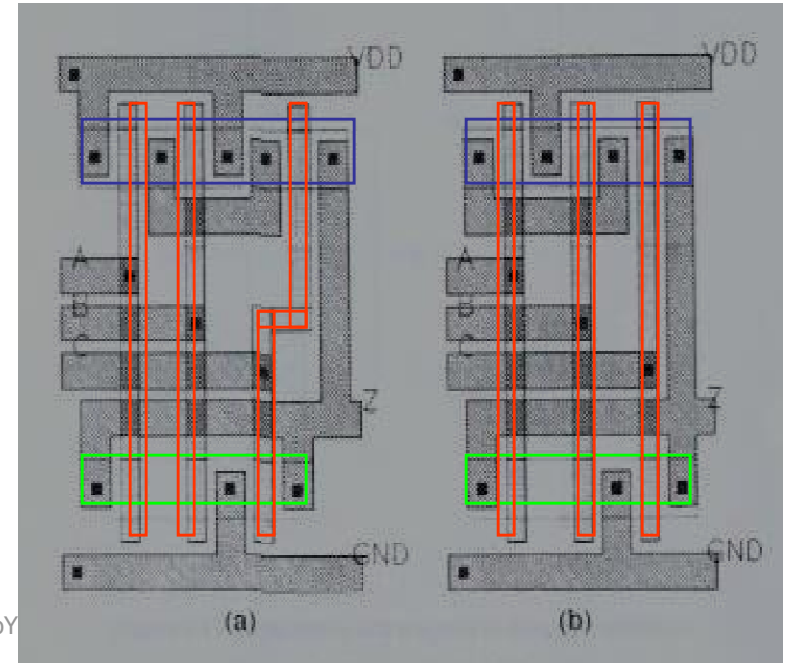
(b) 版图

门电路版图——6. CMOS AOI门

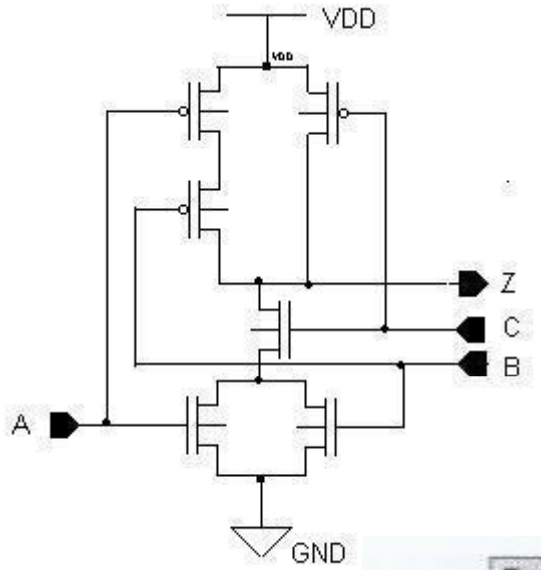


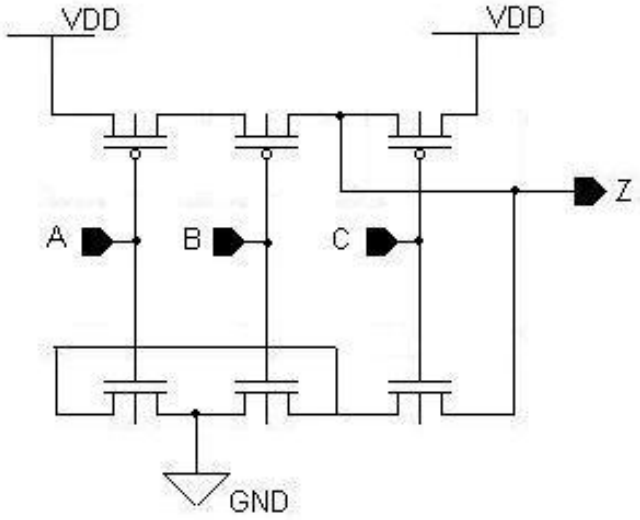


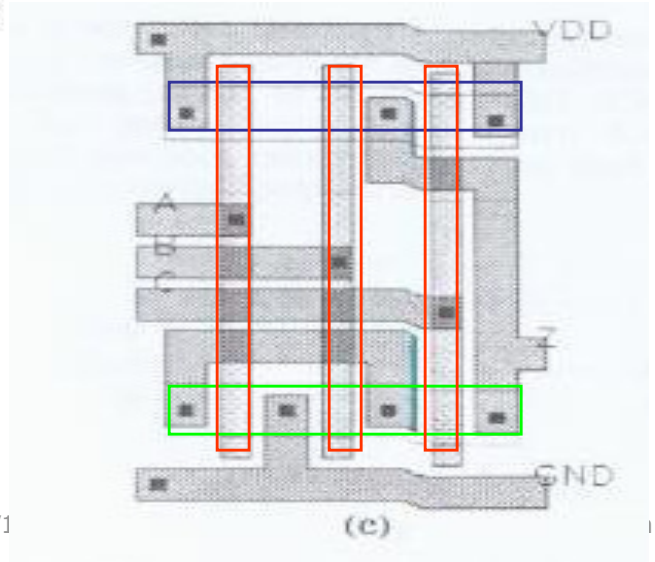




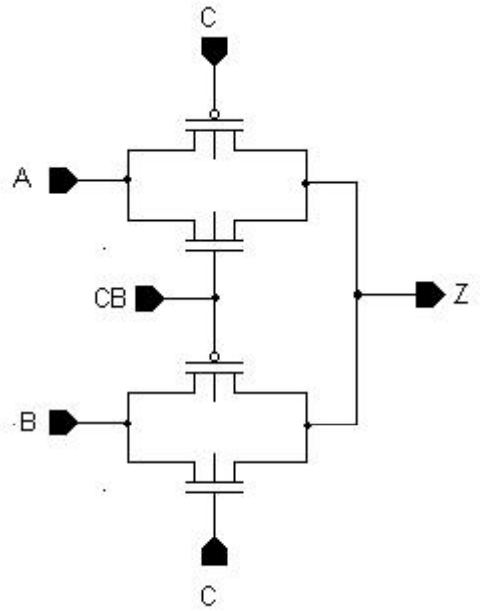
门电路版图——7. CMOS OAI门

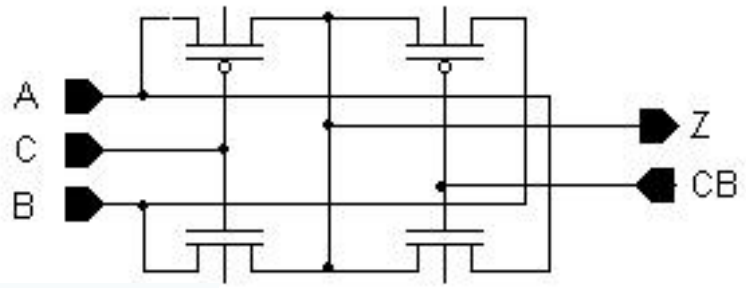


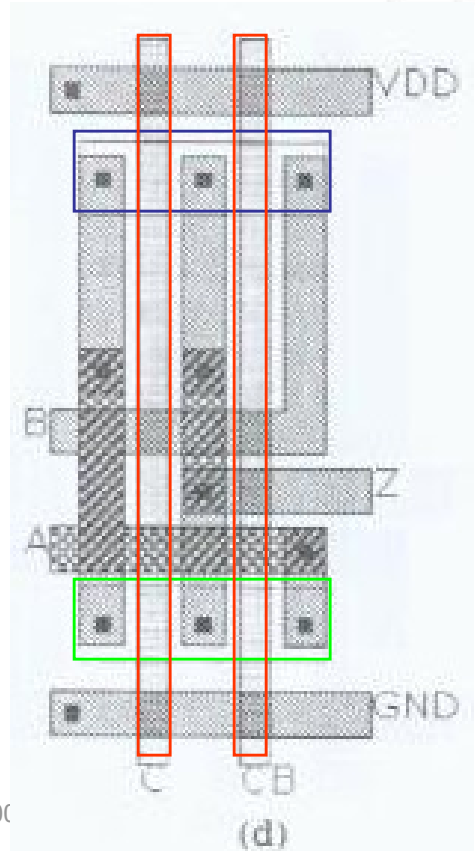




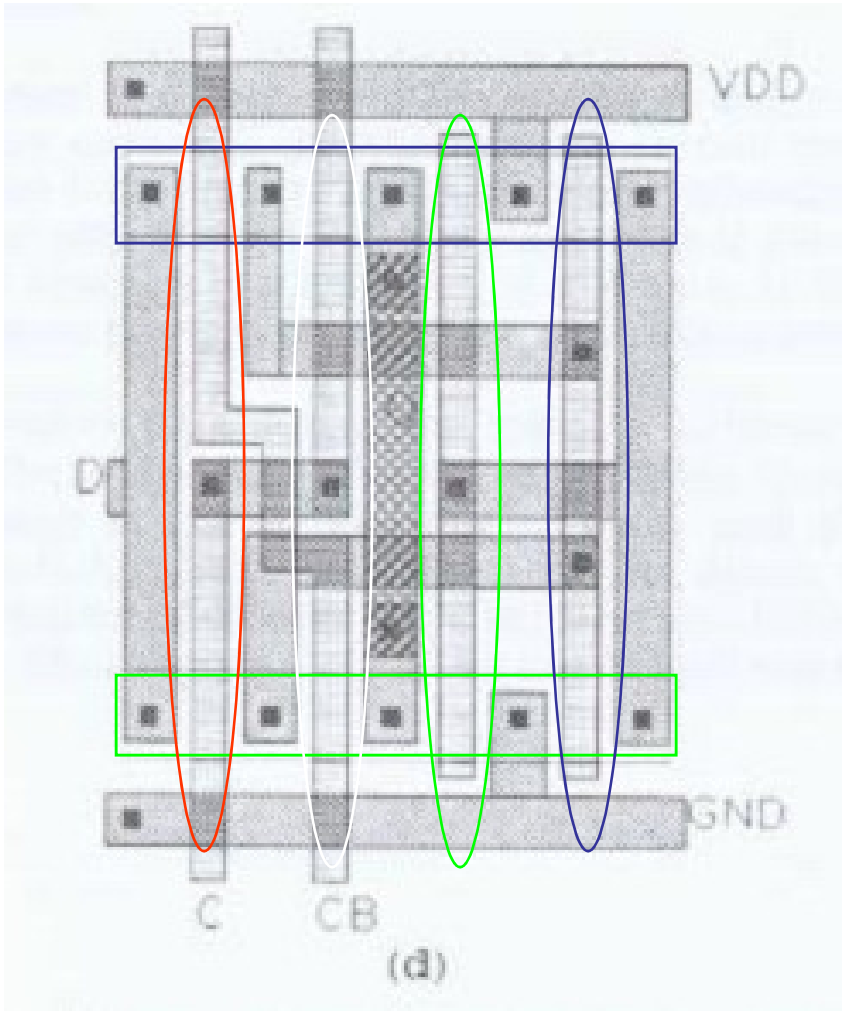
门电路版图——8. 2输入选择器

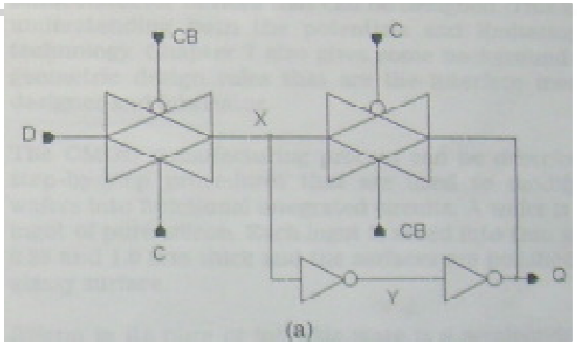


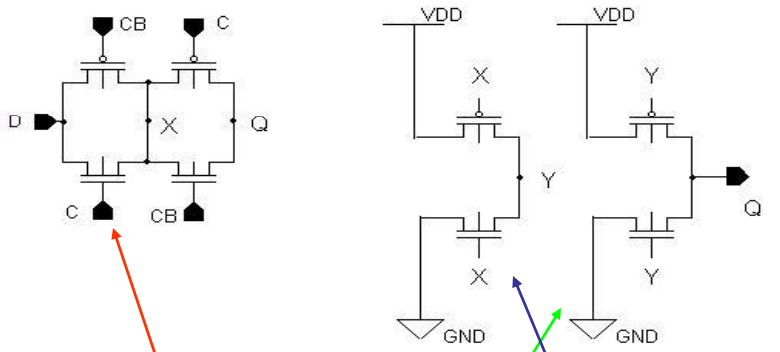


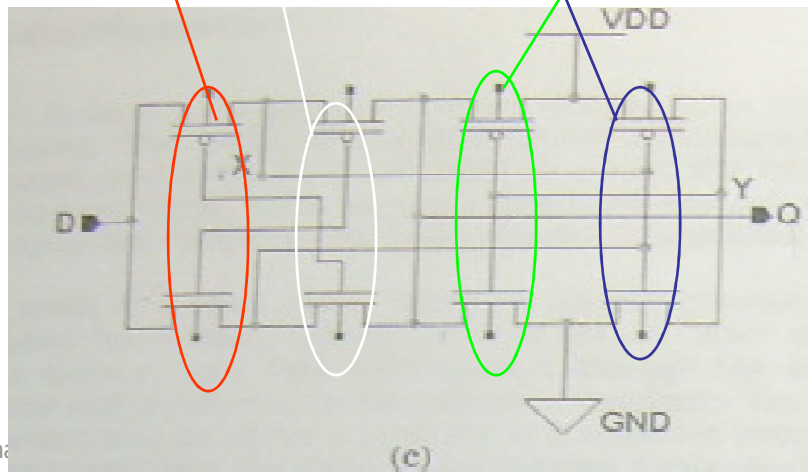


门电路版图——9. CMOS触发器

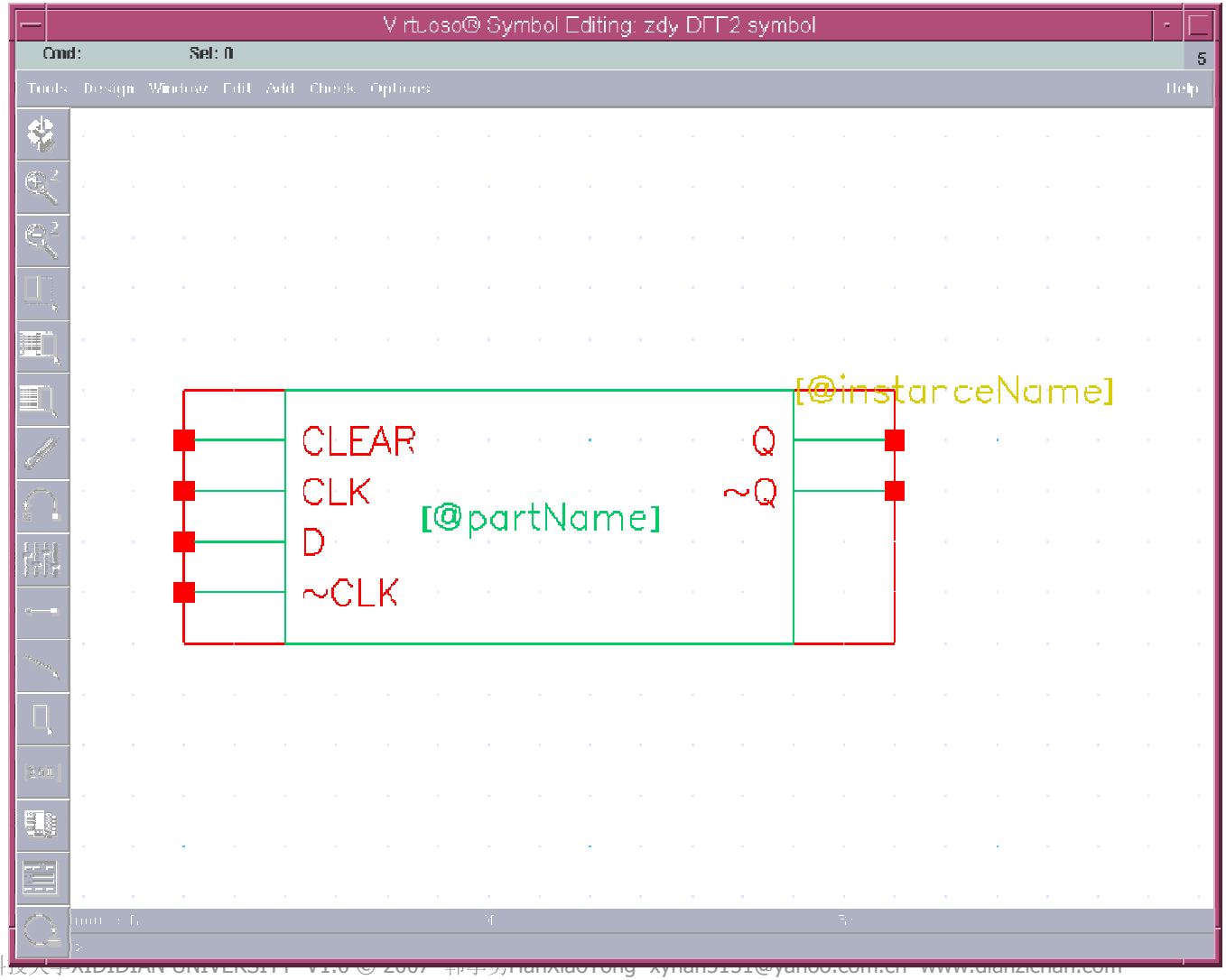




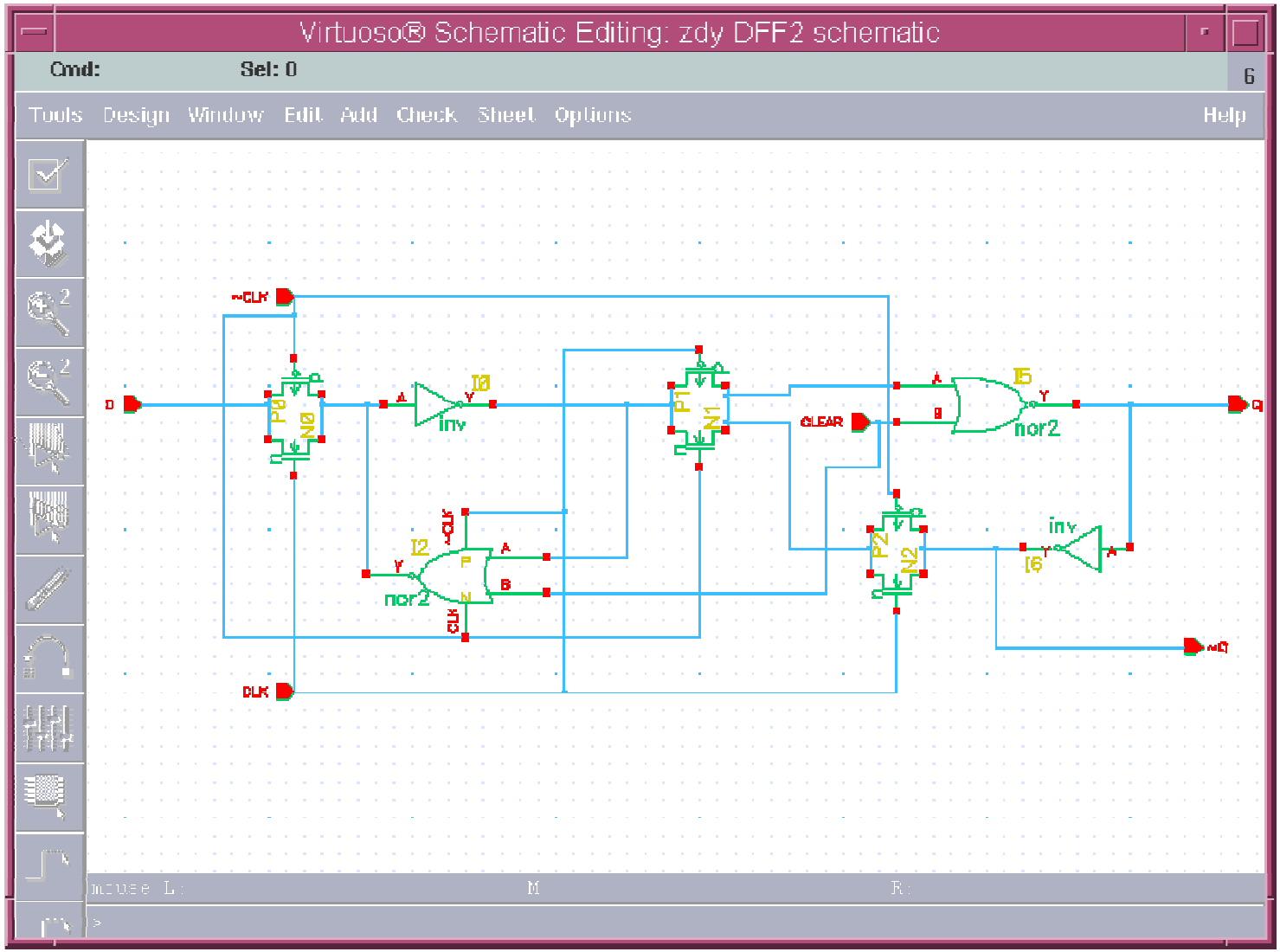




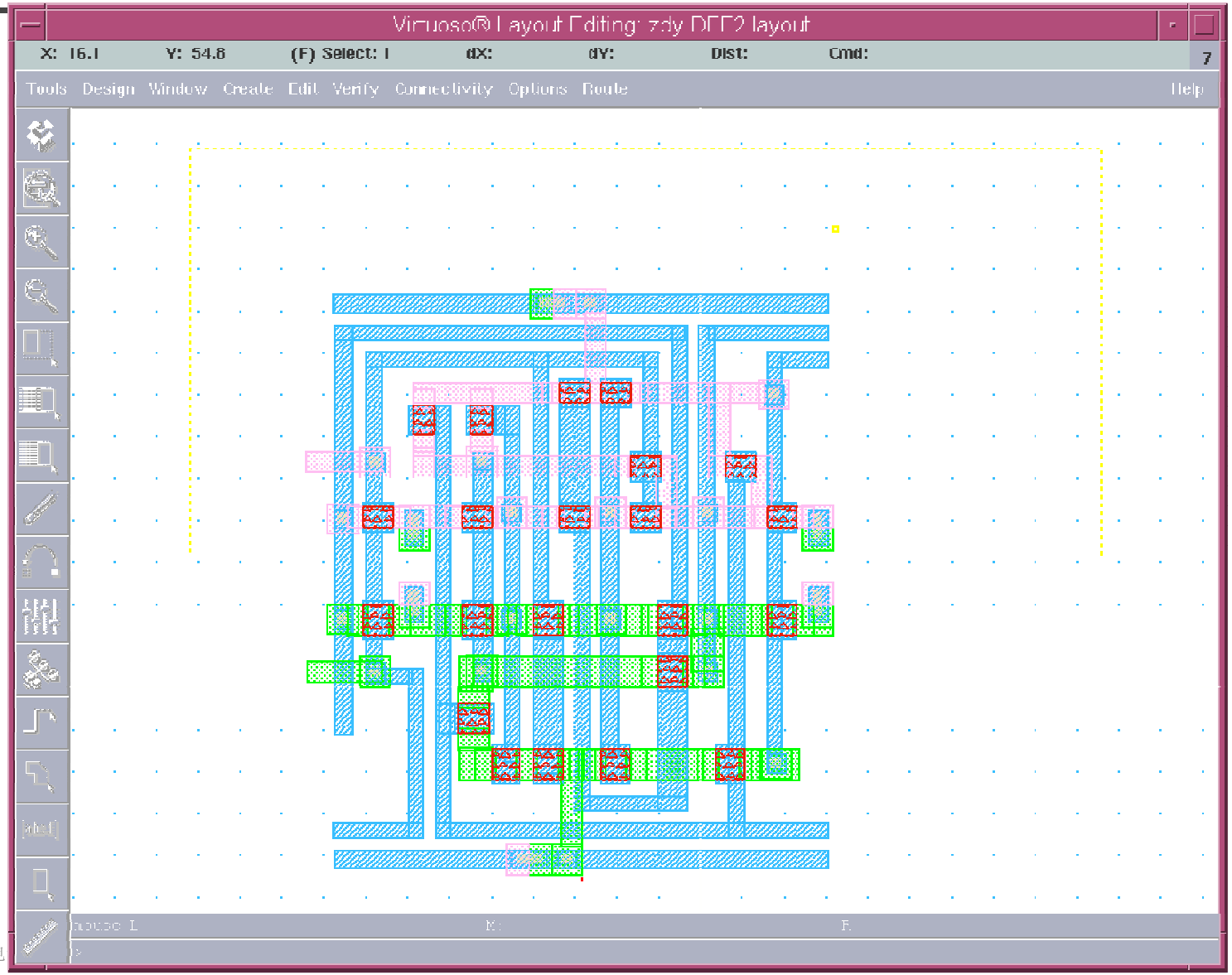
门电路版图——9. CMOS触发器



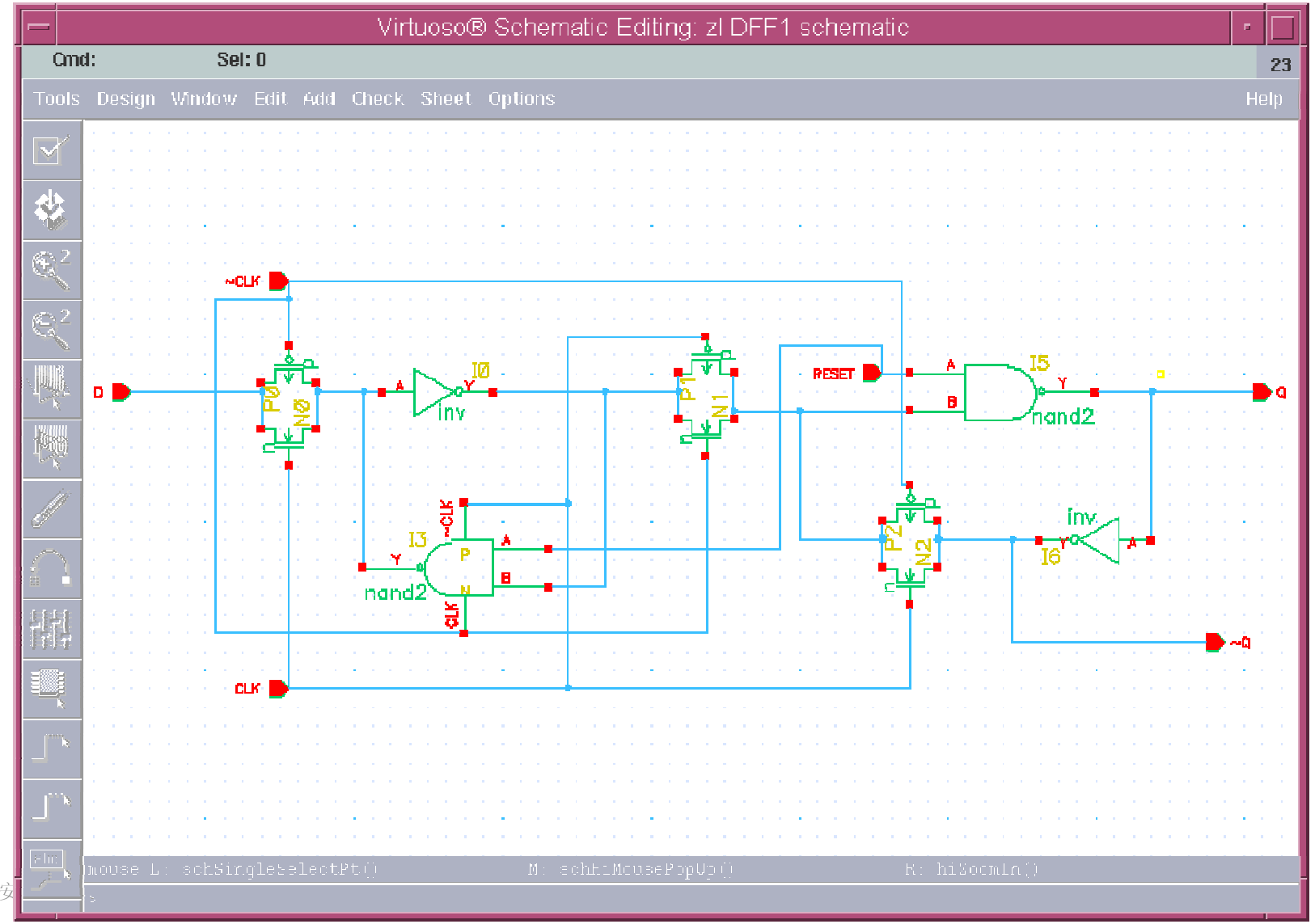
门电路版图——9. CMOS触发器



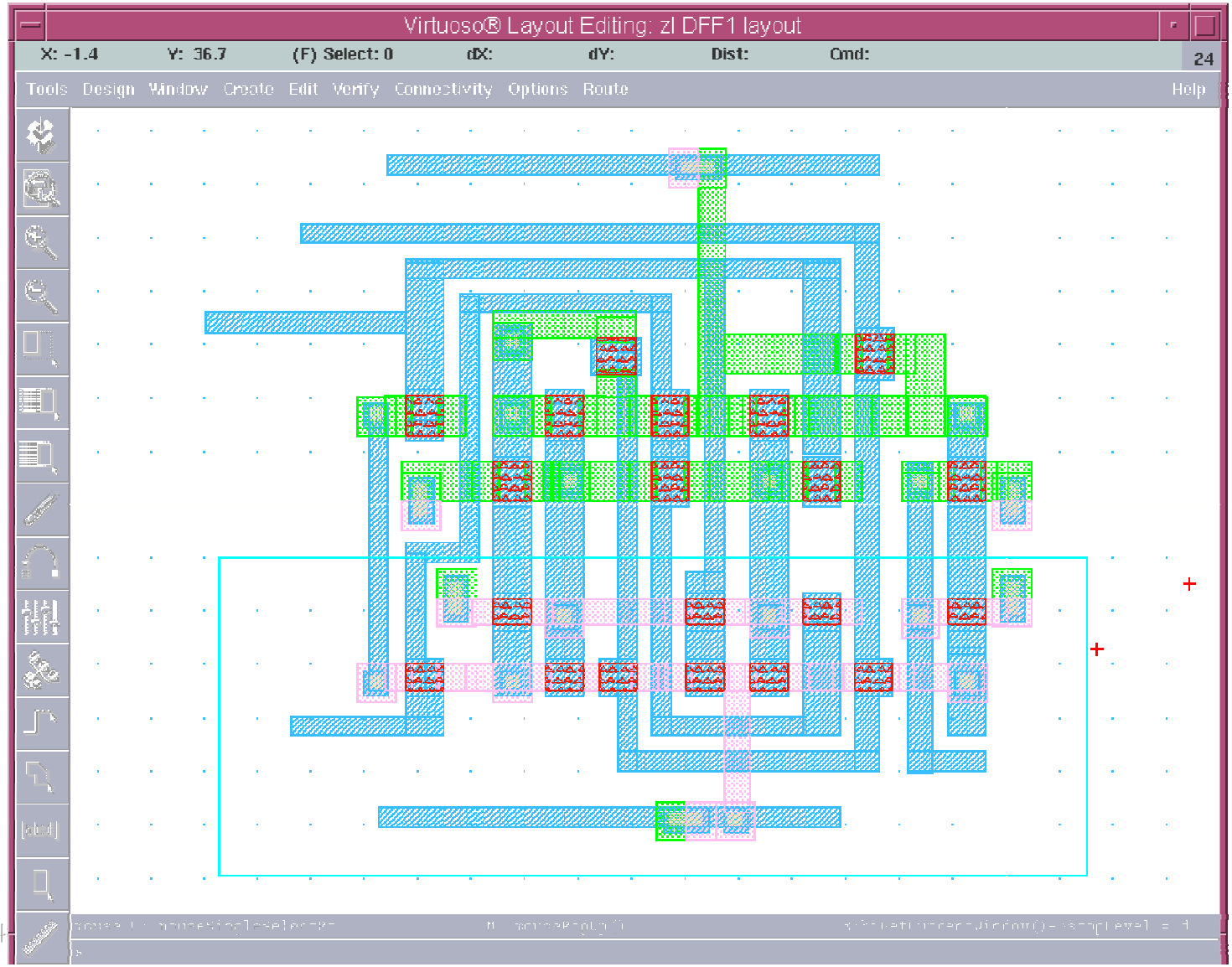
门电路版图——9. CMOS触发器



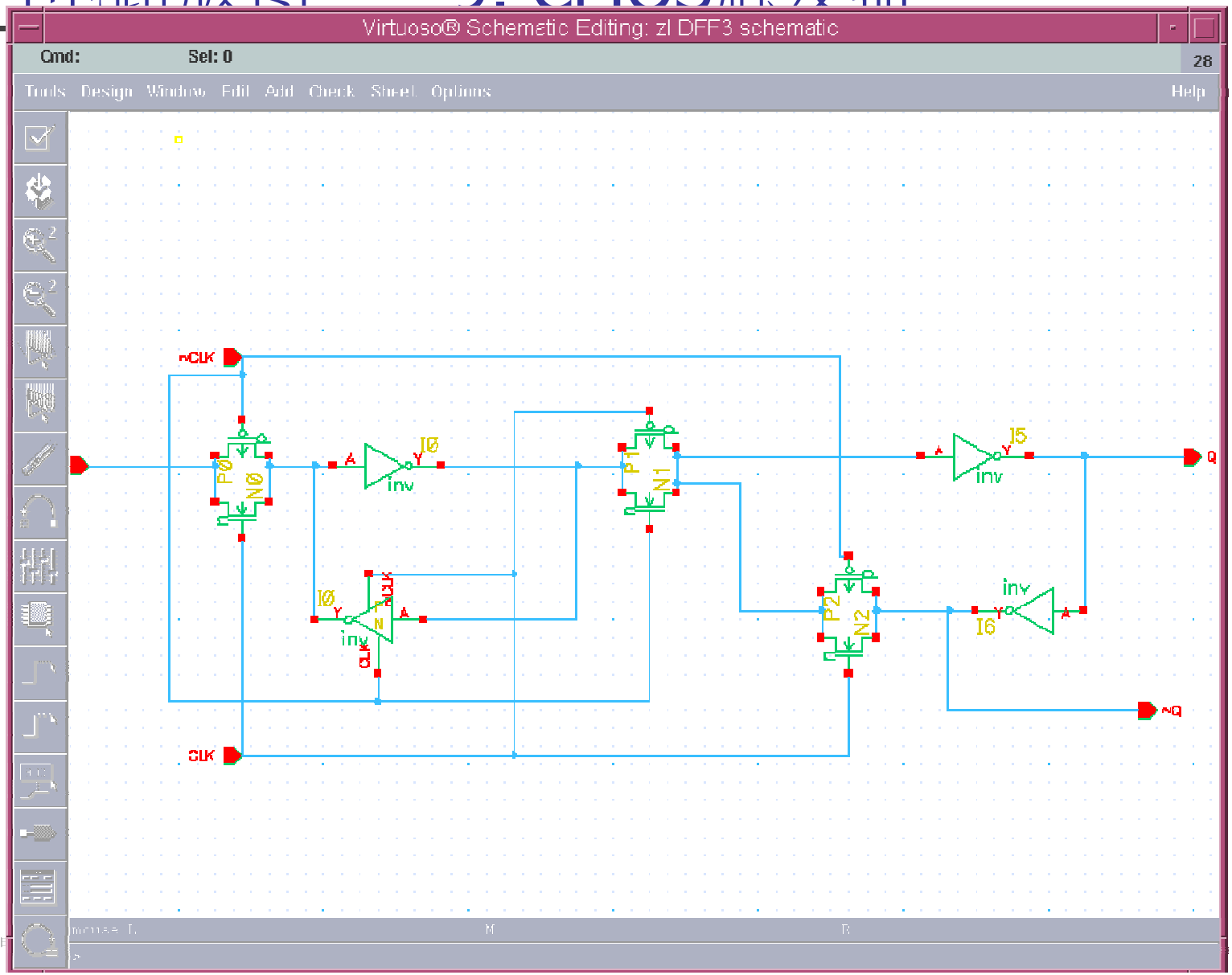
门电路版图——9. CMOS触发器



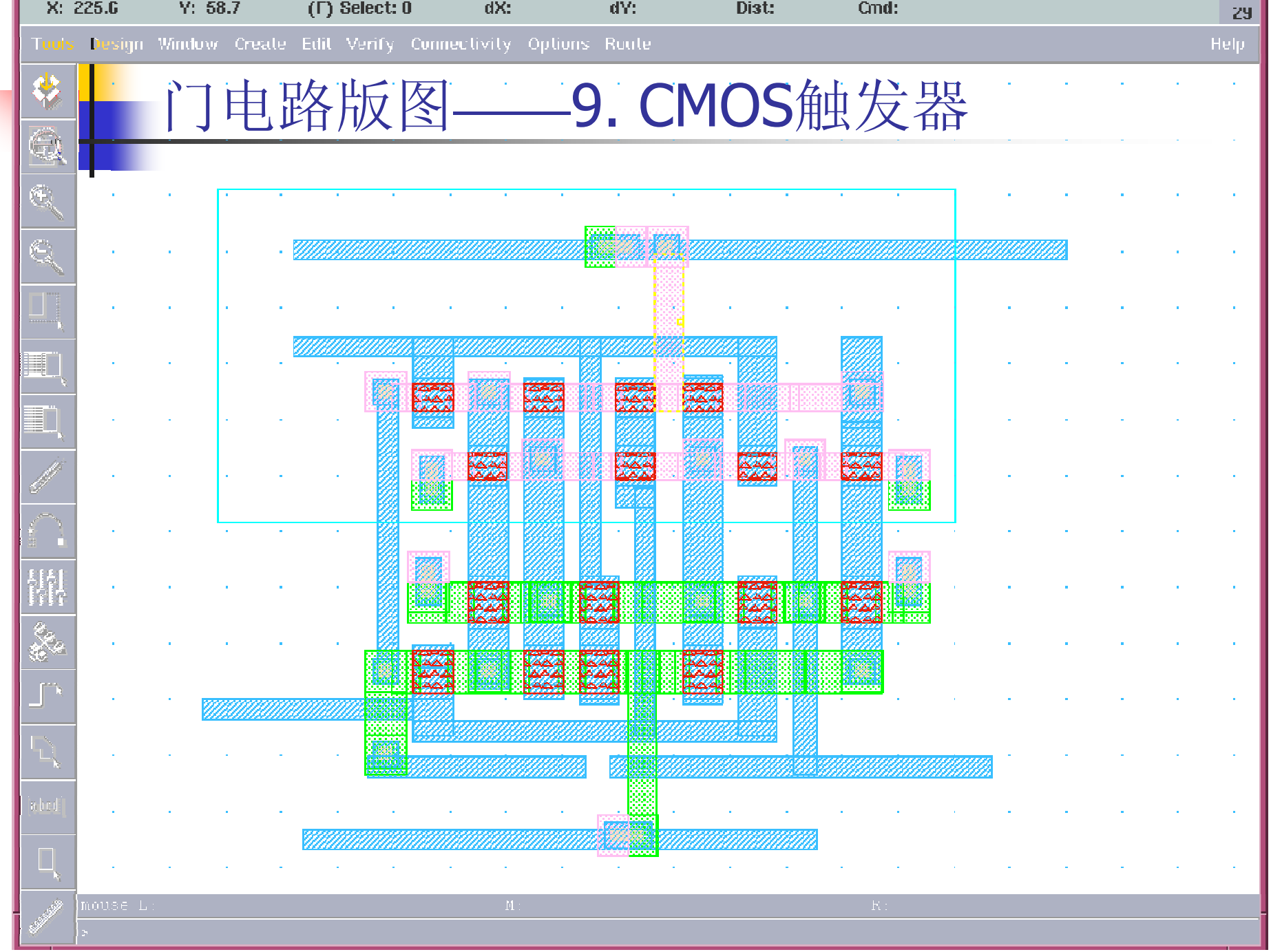
门电路版图——9. CMOS触发器



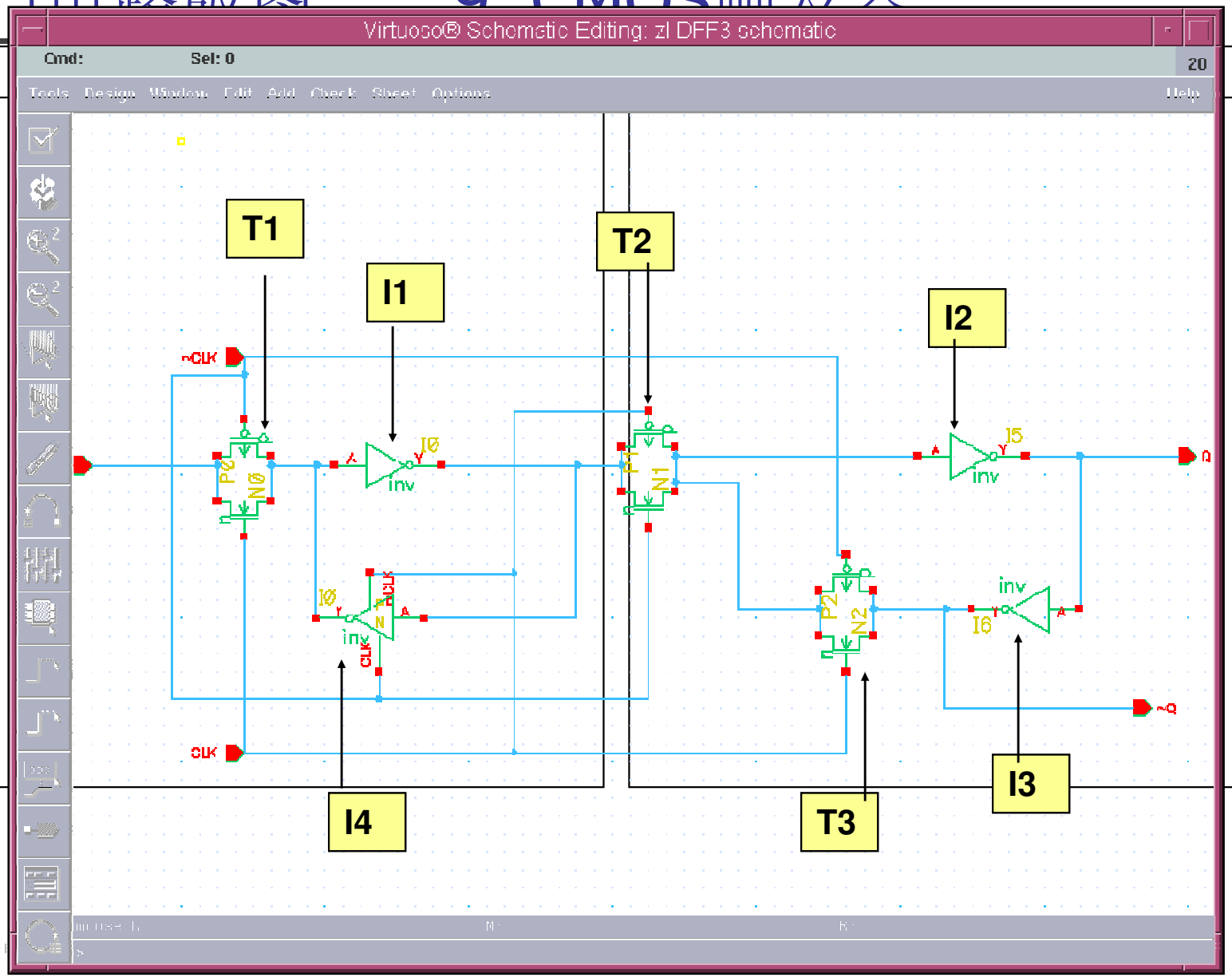
门电路版图——9. CMOS触发器

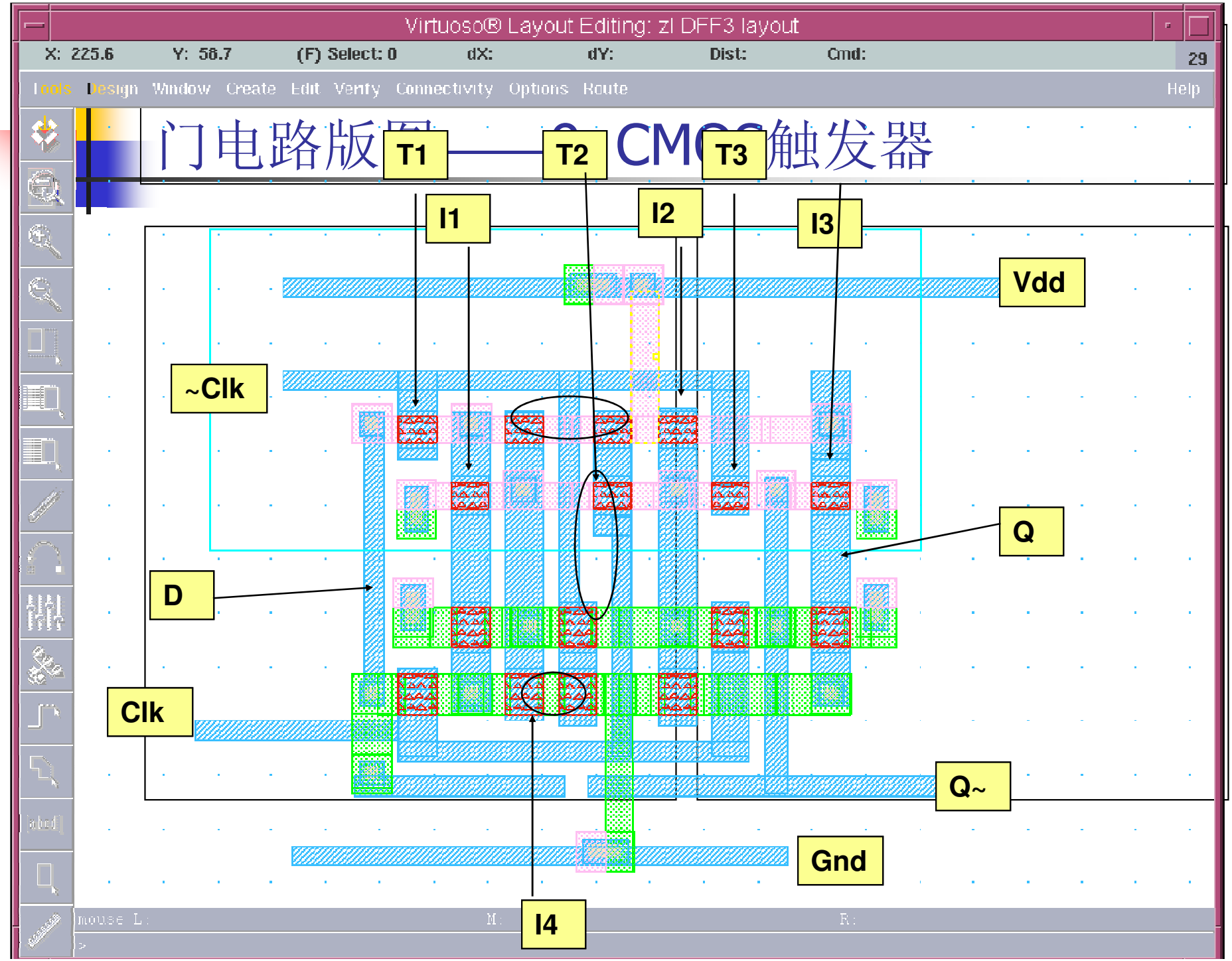


门电路版图——9. CMOS触发器



门电路版图 9 CMOS触发器

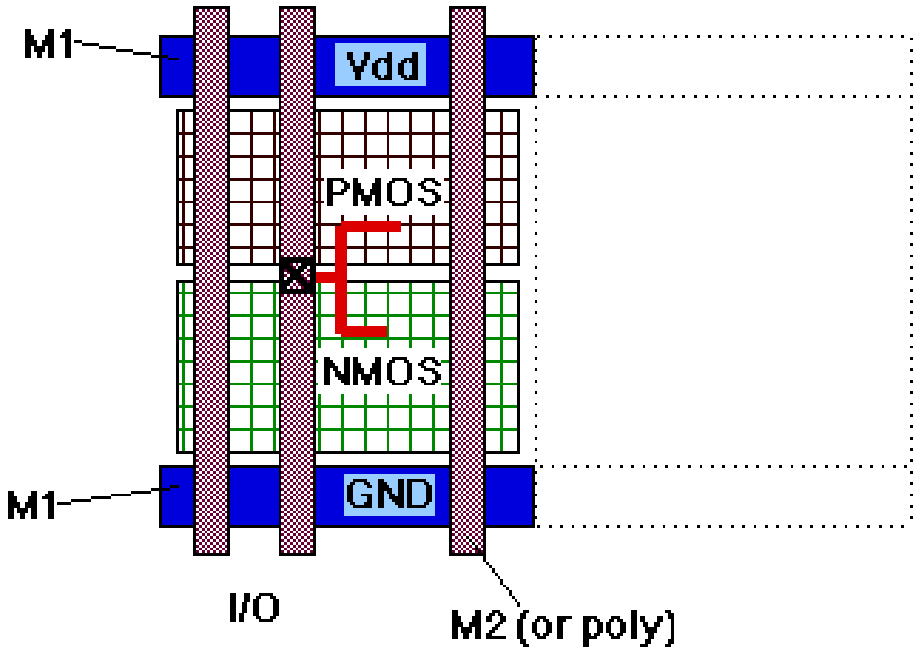



Virtuoso® Layout Editing: zl DFF3 layout
X: 225.6
Y: 58.7
(F) Select: 0
dX:
dY:
Dist:
Cmd:
29
Tools Design Window Create Edit Verify Connectivity Options Route Help
门电路版图——2-CMOS触发器
T1
T2
T3
I1
I2
I3
Vdd
~Clk
Q
D
Clk
Q~
Gnd
I4
mouse L:
M:
R:

标准单元版图

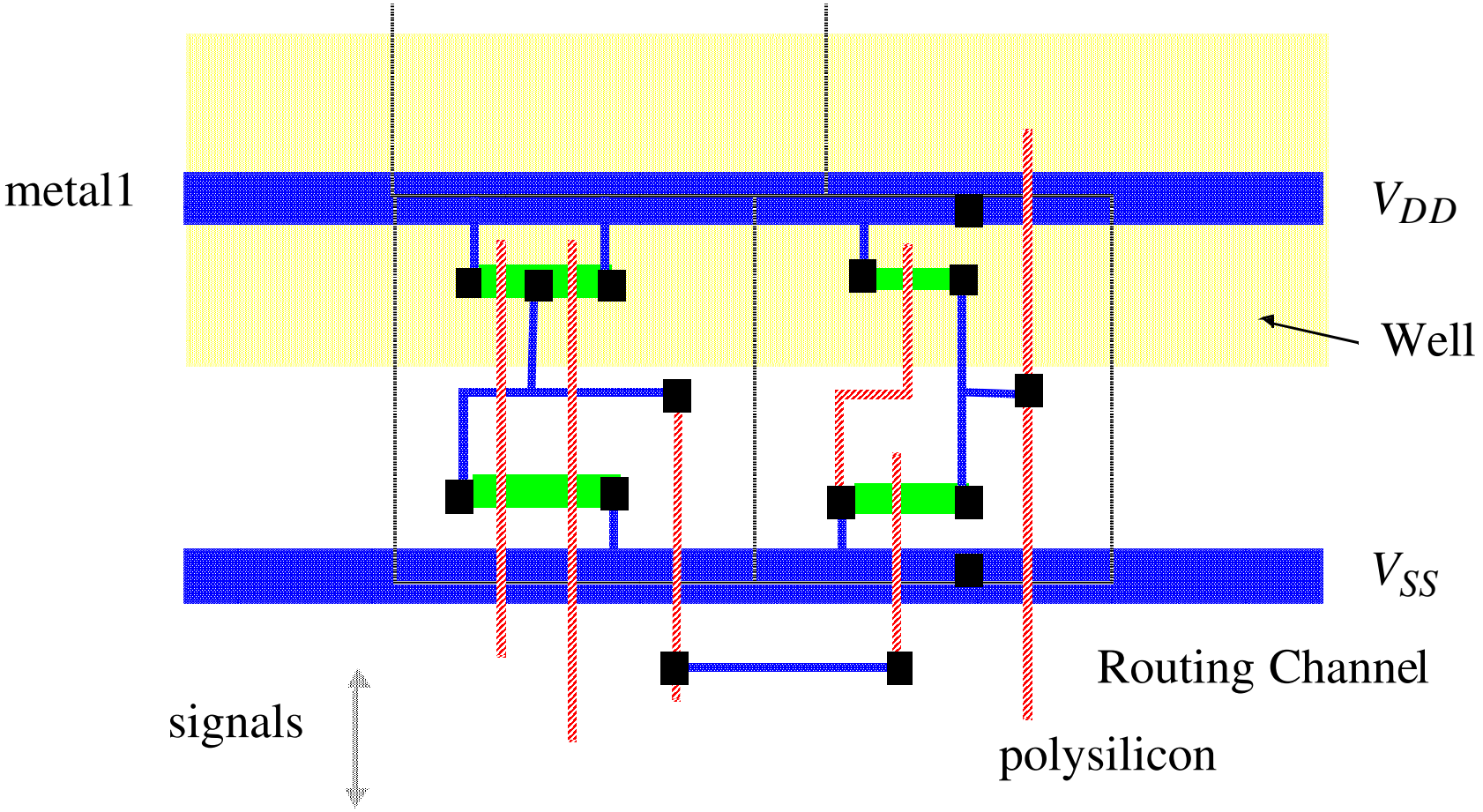
什么是标准单元？

- Standard Cell
  - 等高不等宽
  - 有输入、输出、V_{DD}、GND（V_{SS}）四类端口
  - 可繁可简：可以是单个FET，也可以是算术运算单元ALU
  - 内部设计完全符合设计规则



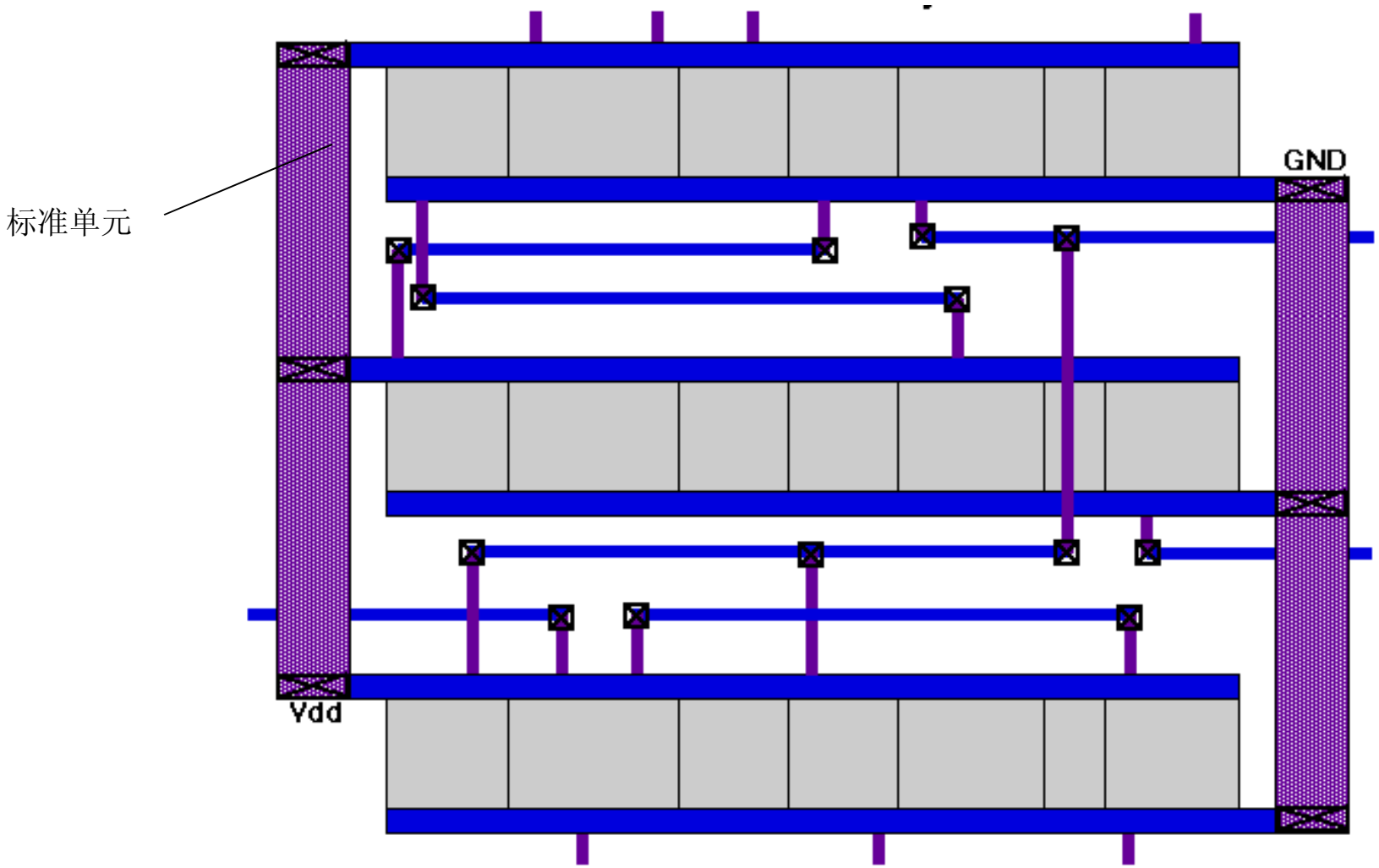
标准单元版图

标准单元内部布局

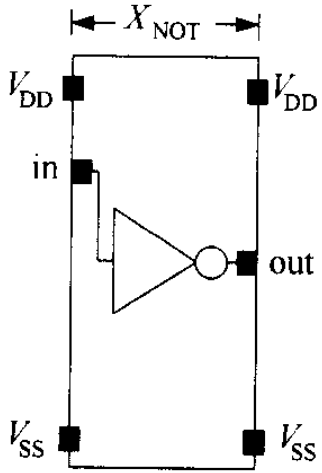


标准单元版图

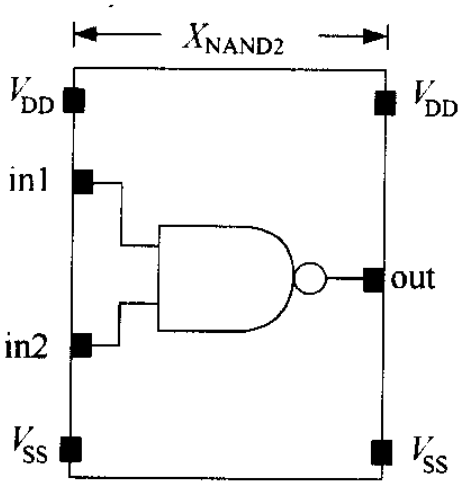
标准单元外部布局



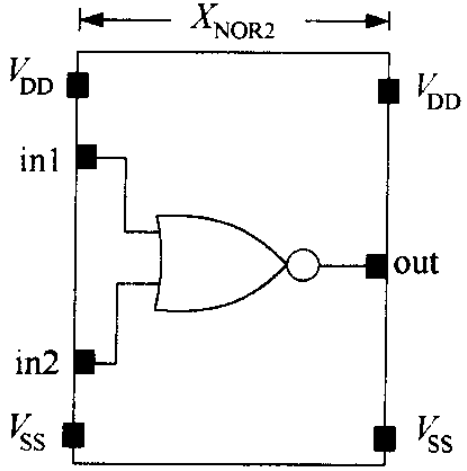
标准单元版图　作为标准单元的逻辑门



NOT

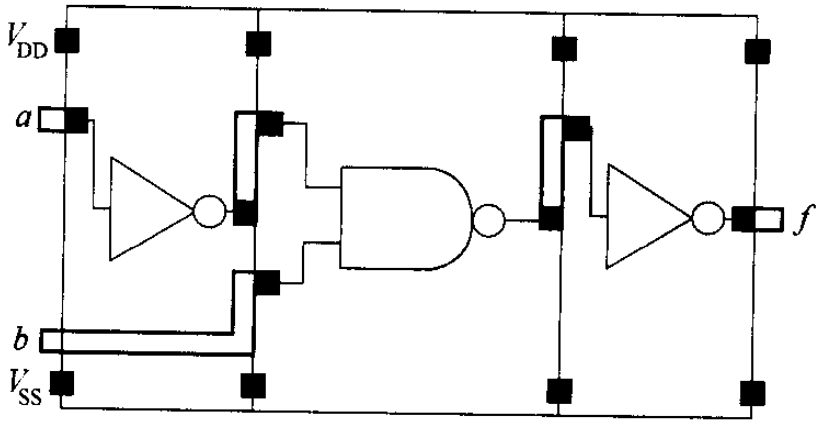


NAND2

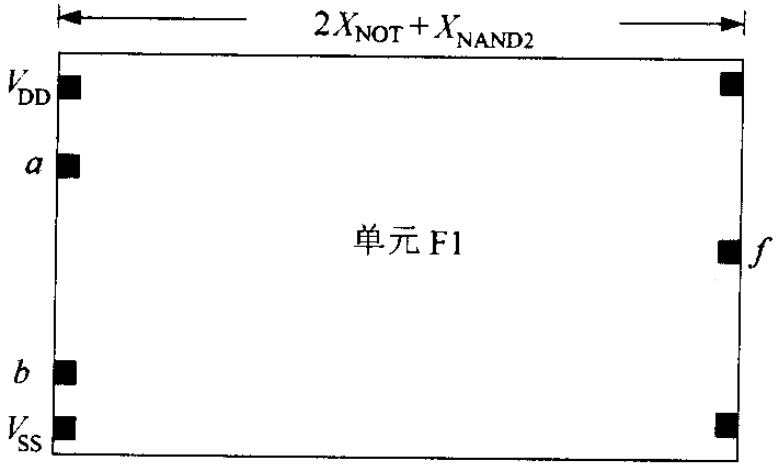


NOR2

标准单元版图　用标准单元构成新单元



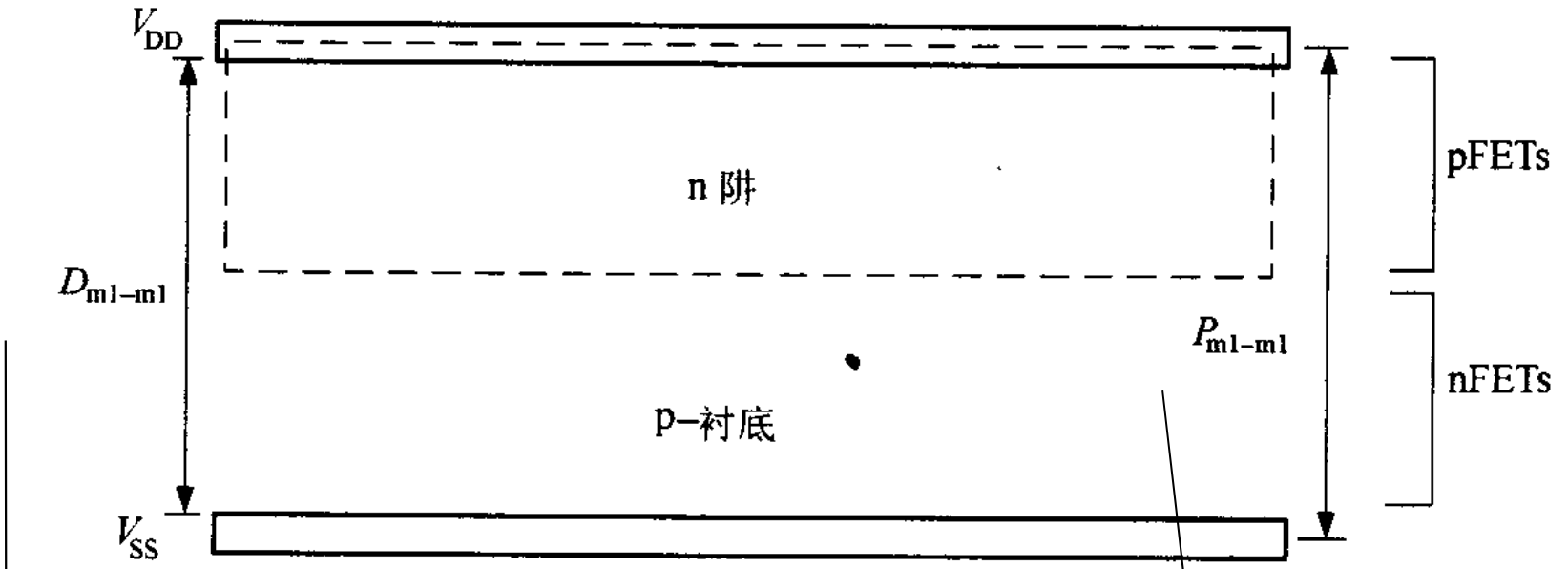
(a) 基本单元



(b) 新的复杂单元

使用者可不必关心内部细节，只知外部特性即可

标准单元版图　　电源线及n阱的位置

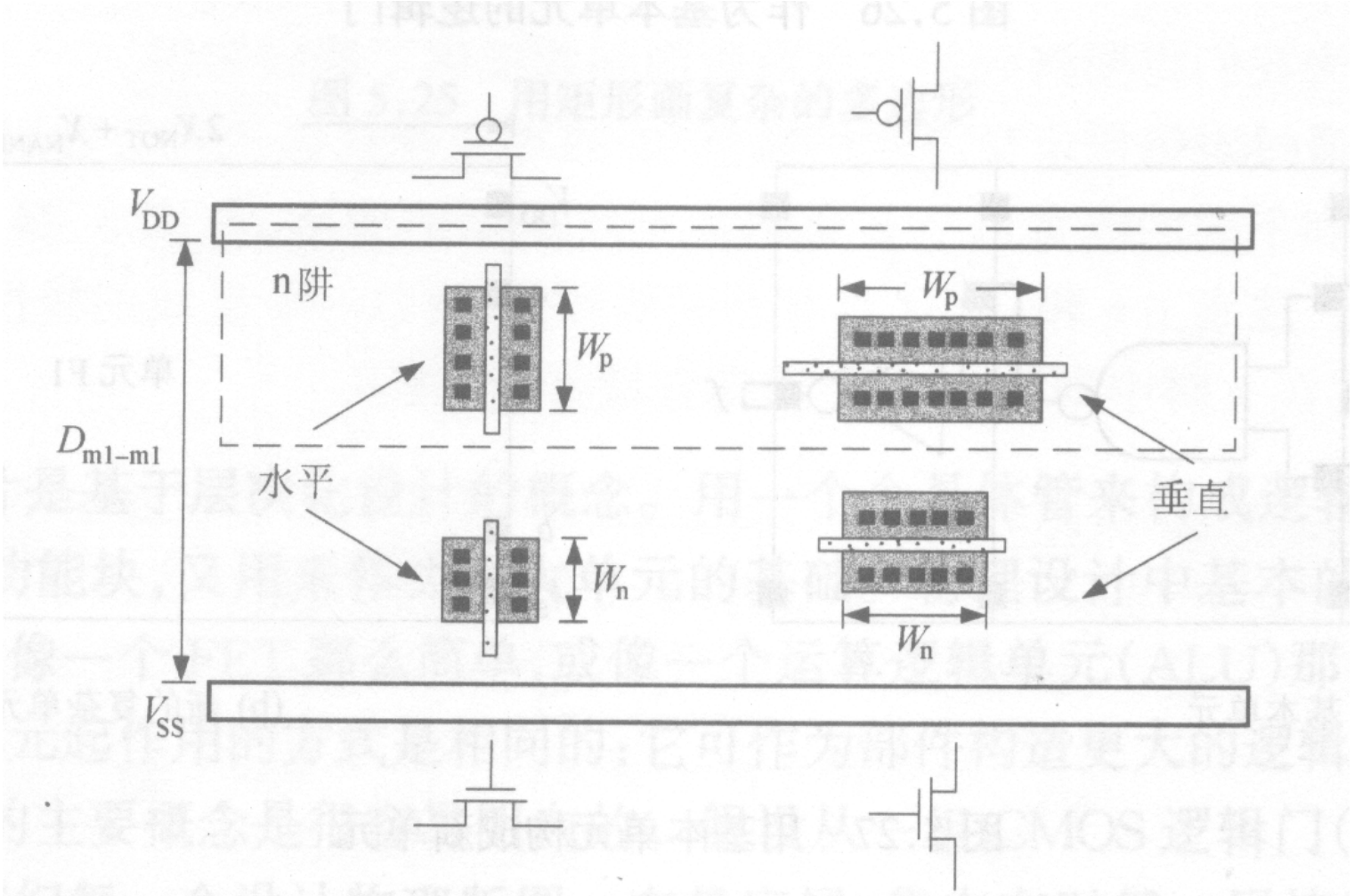


V_{DD}与V_{SS}的边线间距

V_{DD}与V_{SS}的中线间距

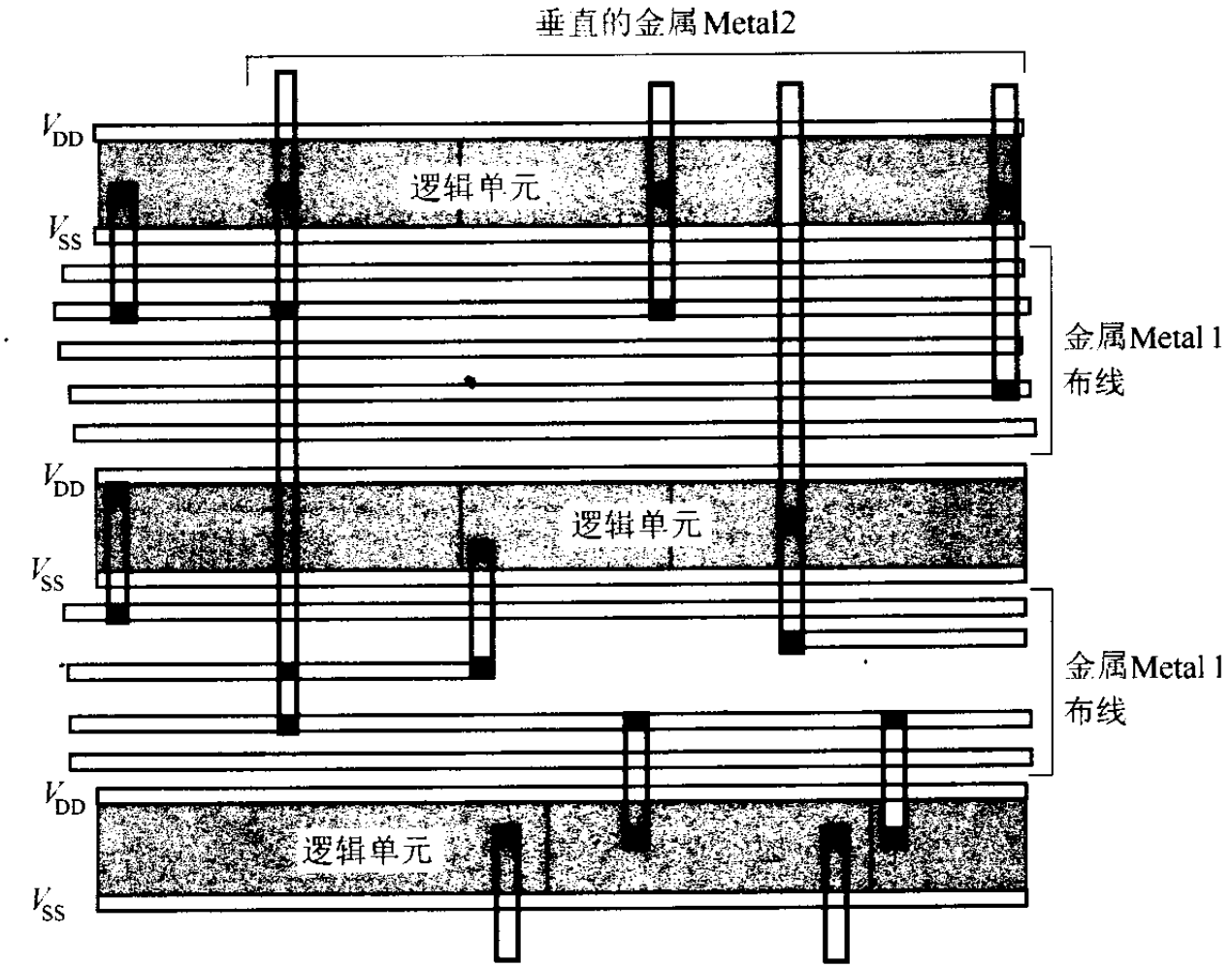
标准单元版图

MOSFET的取向

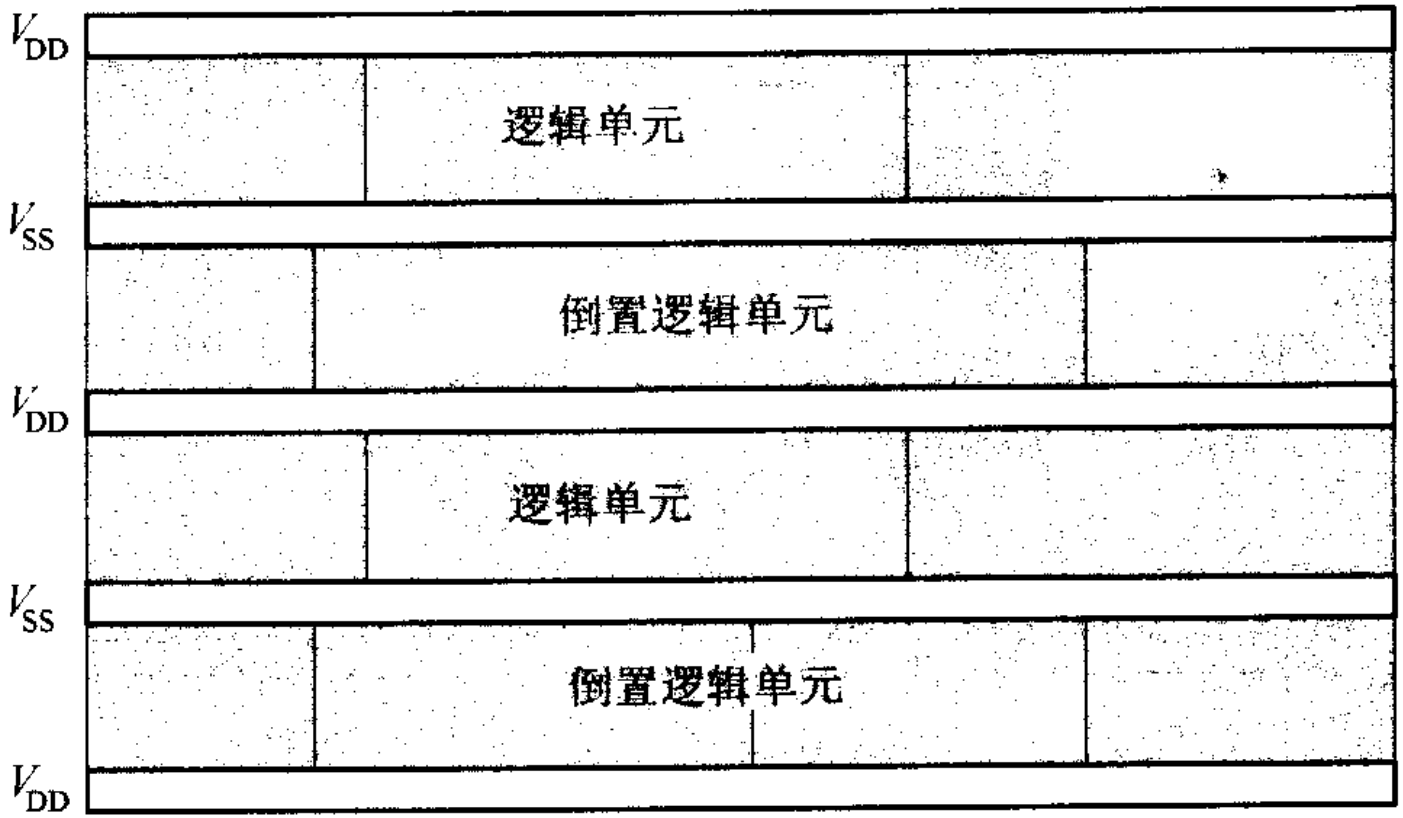


标准单元版图

等高的布线通道



标准单元版图　Weinberger镜像阵列(1)



好处：共用V_{DD}、V_{SS}